32-Bit Proprietary Microcontroller

CMOS

FR60 MB91350A Series

MB91F355A/F356B/355A/354A/V350A

■ DESCRIPTION

The FR families are lines of standard single-chip microcontrollers each based on a 32-bit high-performance RISC CPU, incorporating a variety of I/O resources and bus control features for embedded control applications which require high CPU performance for

This FR60 family is based on FR30 and FR40 families and enhanced is bus access. The FR60 family is a line of single-chip oriented microcontrollers incorporating a wealth of peripheral resources.

The FR60 family is optimized for embedded control applications requiring high processing power of the CPU, such as DVD player, navigation, high performance Fax machine, and printer controls.

■ FEATURES

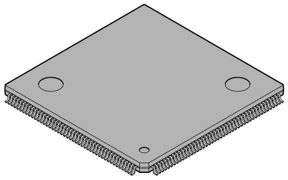
1. FR CPU

- 32-bit RISC, load/store architecture with a five-stage pipeline
- Maximum operating frequency: 50 MHz (using the PLL at an oscillation frequency of 12.5 MHz)
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instruction set optimized for embedded applications: Memory-to-memory transfer, bit manipulation, barrel shift etc.
- Instructions adapted for high-level languages: Function entry/exit instructions, multiple-register load/store instructions

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■ PACKAGE

176-pin plastic LQFP



(FPT-176P-M02)

- Register interlock functions: Facilitating coding in assemblers
- On-chip multiplier supported at the instruction level.
  Signed 32-bit multiplication: 5 cycles.
  Signed 16-bit multiplication: 3 cycles
- Interrupt (PC, PS save): 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- FR family instruction compatible

2. Bus Interface

- Maximum operating frequency: 25 MHz
- Capable of up to 24-bit address full output (16 MB of space)
- 8,16-bit data output
- Built-in pre-fetch buffer
- Non-used data and address pin are usable as general I/O port.
- Capable of chip-select signal output for completely independent four areas settable in 64 KB minimum
- Support for various memory interfaces:
  SRAM, ROM/Flash,
  page mode Flash ROM, page mode ROM
- Basic bus cycle: 2 cycles
- Programmable automatic wait cycle generator capable of inserting wait cycles for each area
- RDY input for external wait cycles
- Support for fly-by transfer for DMA, which enables wait control of independent I/O

3. Mounted Memory

Memory	MB91V350A	MB91F355A	MB91F356B	MB91355A	MB91354A
ROM	No	512 KB	256 KB	512 KB	384 KB
RAM (stack)	16 KB	16 KB	16 KB	16 KB	8 KB
RAM (executable)	16 KB	8 KB	8 KB	8 KB	8 KB

4. DMAC (DMA Controller)

- Capable of simultaneous operation of up to 5 channels (3 channels for external→external operation)
- Three transfer sources (external pin, internal peripheral, software) selectable by software. (Transfer can be started from UART0/1/2.)
- Addressing using 32-bit full addressing mode (increment, decrement, fixed)
- Transfer modes (demand transfer, burst transfer, step transfer, block transfer)
- Support for fly-by transfer (between external I/O and memory)
- Selectable transfer data size: 8, 16, or 32-bit
- Multi-byte transfer enabled (by software)
- DMAC descriptor in IO areas (200_H to 240_H, 1000_H to 1024_H)

5. Bit Search Module (for REALOS)

- Search for the position of the bit 1/0-changed first in 1 word from the MSB

6. Various Timers

- 4 channels of 16-bit reload timer (including 1 channel for REALOS):
  Internal clock frequency selectable from among divisions by 2/8/32 (division by 64/128 selectable only for ch3)
- 16-bit free-running timer: 1 channel.
  Output compare module: 8 channels. Input capture module: 4 channels
- 16-bit PPG timer 6 channels

7. UART

- UART Full duplex double buffer 5 channel
- Selectable parity On/Off
- Asynchronous (start-stop synchronized) or CLK-synchronous communications selectable

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- Internal timer for dedicated baud rate
- External clock can be used as transfer clock
- Assorted error detection functions (for parity, frame, and overrun errors)
- 115 Kbps support

8. SIO

- 3 channels for 8-bit data serial transfer
- Shift clock selectable from among internal three and external one
- Shift direction selectable (transfer from LSB or MSB) selectable

9. Interrupt Controller

- Total of 17 external interrupt lines (1 nonmaskable interrupt pin and 16 normal interrupt pins available for Wake Up from STOP)
- interrupt from internal peripheral
- Programmable priorities (16 levels) for all interrupts except the non-maskable interrupt

10. D/A Converter

- 8-bit resolution. 3 channels

11. A/D Converter

- 10-bit resolution. 12 channels
- Casting time for serial/parallel conversion: 1.48 µs
- Conversion mode (single conversion mode, continuous conversion mode)
- Activation source (software, external trigger, peripheral interrupt)

12. Other Interval Timer/Counter

- 8/16-bit up/down counter
- 16-bit PPG timer 5 channels
- Watch dog timer

13. I²C Bus Interface (400 Kbps supported)

- 1channel master/slave sending and receiving
- Arbitration and clock synchronization

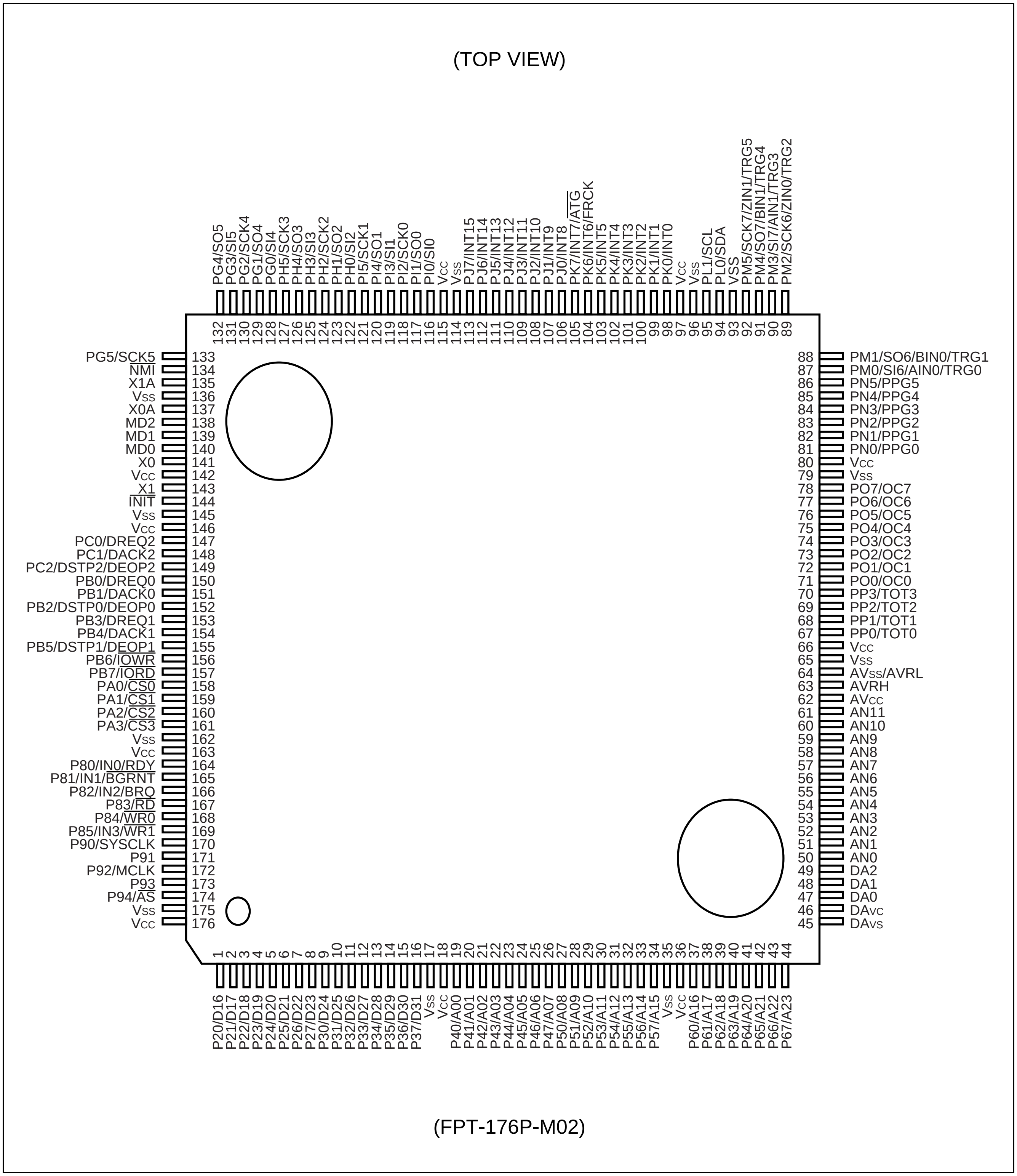
14. I/O Port

- 3 V I/O ports (16 ports shared for external interrupts support 5 V input.)
- Max 126 ports

15. Other Features

- Internal oscillator circuit as clock source, allowing PLL multiplication to be selected
- Provided with $\overline{\text{INIT}}$ as a reset pin (The CPU operates without oscillation stabilization wait interval when the $\overline{\text{INIT}}$ pin is reset.)
- others, watch-dog timer reset, software reset enable
- Support for stop and sleep modes for low power consumption, capable of saving power during CPU operation at 32 kHz.
- Gear function
- Built-in time base timer
- Package: LQFP-176 (lead pitch: 0.50 mm)
- CMOS technology(0.35 µm)
- Power supply voltage: 3.3 V ± 0.3 V

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Description
1 to 8	D16 to D23	C	External data bus bit 16 to bit 23. Enabled in external bus mode.
	P20 to P27		Available as a port in external bus 8-bit mode.
9 to 16	D24 to D31	C	external data bus bit 24 to bit 31. Enabled in external bus mode.
	P30 to P37		Usable as port at single chip mode.
19 to 26	A00 to A07	C	Bits 0 to 7 of external address bus. Enabled in external bus mode.
	P40 to P47		Usable as port at single chip mode.
27 to 34	A08 to A15	C	Bits 8 to 15 of external address bus. Enabled in external bus mode.
	P50 to P57		Usable as port at single chip mode.
37 to 41	A16 to A20	C	Bits 16 to 20 of external address bus. Enabled in external bus mode.
	P60 to P64		Available as a port either in single chip mode or with no external address bus in use.
42 to 44	A21 to A23	C	Bits 21 to 23 of external address bus. Enabled in external bus mode.
	P65 to P67		Available as a port either in single chip mode or with no external address bus in use.
47 to 48	DA0, DA1	—	D/A converter output pin.
49	DA2	—	D/A converter output pin.
50 to 57	AN0 to AN7	G	Analog input pin.
58 to 61	AN8 to AN11	G	Analog input pin.
67 to 70	TOT0 to TOT3	D	Reload timer output port. This function is enabled when timer output is enabled.
	PP0 to PP3		General purpose input/output port. This function is enabled when the timer output function is disabled.
71	OC0	D	Output compare pin.
	PO0		General purpose I/O. This function is available as a port when the output compare output is not in use.
72	OC1	D	Output compare pin.
	PO1		General purpose I/O. This function is available as a port when the output compare output is not in use.
73	OC2	D	Output compare pin.
	PO2		General purpose I/O. This function is available as a port when the output compare output is not in use.
74 to 78	OC3 to OC7	D	Output compare pin.
	PO3 to PO7		General purpose I/O. This function is available as a port when the output compare output is not in use.
81	PPG0	D	PPG timer output pin.
	PN0		General purpose I/O. This function is available as a port when the PPG timer output is not in use.

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Pin no.	Pin name	Circuit type	Description
82	PPG1	D	PPG timer output pin.
	PN1		General purpose I/O. This function is available as a port when the PPG timer output is not in use.
83	PPG2	D	PPG timer output pin.
	PN2		General purpose I/O. This function is available as a port when the PPG timer output is not in use.
84	PPG3	D	PPG timer output pin.
	PN3		General purpose I/O. This function is available as a port when the PPG timer output is not in use.
85	PPG4	D	PPG timer output pin.
	PN4		General purpose I/O. This function is available as a port when the PPG timer output is not in use.
86	PPG5	D	PPG timer output pin.
	PN5		General purpose I/O. This function is available as a port when the PPG timer output is not in use.
87	SI6	D	Data input for serial I/O6. Since this input is used as required when serial I/O 6 is in input operation, the port output must remain off unless intentionally turned on.
	AIN0		8/16-bit up/down counter input. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
	TRG0		External trigger input for PPG timer0. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
	PM0		General purpose I/O. This function is available a port when the serial I/O, 8/16-bit up/down counter, and PPG timer outputs are not in use.
88	SO6	D	Data output for serial I/O 6. This function is enabled when the serial I/O6 data output is enabled.
	BIN0		8/16-bit up/down counter input. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
	TRG1		External trigger input for PPG timer1. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
	PM1		General purpose I/O. This function is available a port when the serial I/O, 8/16-bit up/down counter, and PPG timer outputs are not in use.
89	SCK6	D	Clock input/output for serial I/O 6. This function is enabled when serial I/O6 is using the external shift clock mode, or serial I/O5 clock output function is enabled.
	ZIN0		8/16-bit up/down counter input. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
	TRG2		External trigger input for PPG timer2. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
	PM2		General purpose I/O. This function is available a port when the serial I/O, 8/16-bit up/down counter, and PPG timer outputs are not in use.

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Pin no.	Pin name	Circuit type	Description
90	SI7	D	Data input for serial I/O 7. Since this input is used as required when serial I/O 7 is in input operation, the port output must remain off unless intentionally turned on.
90	AIN1	D	8/16-bit up/down counter input. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
90	TRG3	D	External trigger input for PPG timer 3. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
90	PM3	D	General purpose I/O. This function is available a port when the serial I/O, 8/16-bit up/down counter, and PPG timer outputs are not in use.
91	SO7	D	Data output for serial I/O 7. This function is enabled when the serial I/O 7 data output is enabled.
91	BIN1	D	8/16-bit up/down counter input. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
91	TRG4	D	External trigger input for PPG timer 4. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
91	PM4	D	General purpose I/O. This function is available a port when the serial I/O, 8/16-bit up/down counter, and PPG timer outputs are not in use.
92	SCK7	D	Clock input/output for serial I/O5. This function is enabled when serial I/O 7 is using the external shift clock mode, or serial I/O 5 clock output function is enabled.
92	ZIN1	D	8/16-bit up/down counter input. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
92	TRG5	D	External trigger input for PPG timer 5. Since this input is used as required when enabled, the port output must remain off unless intentionally turned on.
92	PM5	D	General purpose I/O. This function is available a port when the serial I/O, 8/16-bit up/down counter, and PPG timer outputs are not in use.
94	SDA	F	Clock input/output pin for I²C bus. This function is enabled when the I²C system is enabled for operation in standard mode. The port output must remain off unless intentionally turned on. (Open drain input)
94	PL0	F	General purpose input/output port. This function is available as a port when the I²C system is disabled for operation. (Open drain input)
95	SCL	F	Clock input/output pin for I²C bus. This function is enabled when the I²C system is enabled for operation in standard mode. The port output must remain off unless intentionally turned on. (Open drain input)
95	PL1	F	General purpose input/output port. This function is available as a port when the I²C system is disabled for operation. (Open drain input)
98 to 103	INT0 to INT5	E	External interrupt input. Since this input is used as required when the corresponding external interrupt is enabled, the port output must remain off unless intentionally turned on.
98 to 103	PK0 to PK5	E	General purpose input/output port.

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Pin no.	Pin name	Circuit type	Description
104	INT6	E	External interrupt input. Since this input is used as required when the corresponding external interrupt is enabled, the port output must remain off unless intentionally turned on.
	FRCK		External clock input pin for freerun timer. Since this input is used as required when selected as the external clock input for the free running timer, the port output must remain off unless intentionally turned on.
	PK6		General purpose input/output port.
105	INT7	E	External interrupt input. Since this input is used as required when the corresponding external interrupt is enabled, the port output must remain off unless intentionally turned on.
	$\overline{\text{ATG}}$		External trigger input for A/D converter. Since this input is used as required when selected as an A/D activation source, the port output must remain off unless intentionally turned on.
	PK7		General purpose input/output port.
106 to 113	INT8 to INT15	E	External interrupt input. Since this input is used as required when the corresponding external interrupt is enabled, the port output must remain off unless intentionally turned on.
	PJ0 to PJ7		General purpose input/output port.
116	SI0	D	UART0 data input. Since this input is used as required when UART0 is in input operation, the port output must remain off unless intentionally turned on.
	PI0		General purpose input/output port.
117	SO0	D	UART0 data output. This function is enabled when the UART0 data output is enabled.
	PI1		General purpose input/output port. This function is enabled when the data output function of UART0 is disabled.
118	SCK0	D	UART0 clock input/output pin. This function is enabled either when clock output enabled or when UART0 inputs the external clock signal.
	PI2		General purpose input/output port. This function is enabled when UART0 is not using the external clock signal with the UART0 clock output function disabled.
119	SI1	D	UART1 data input. Since this input is used as required when UART1 is in input operation, the port output must remain off unless intentionally turned on.
	PI3		General purpose input/output port.
120	SO1	D	UART1 data outpu. This function is enabled when the UART1 data output is enabled.
	PI4		General purpose input/output port. This function is enabled when the data output function of UART1 is disabled.
121	SCK1	D	UART1 clock input/output pin. This function is enabled either when clock output enabled or when UART1 inputs the external clock signal.
	PI5		General purpose input/output port. This function is enabled when UART1 is not using the external clock signal with the UART1 clock output function disabled.

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Pin no.	Pin name	Circuit type	Description
122	SI2	D	UART2 data input. Since this input is used as required when UART2 is in input operation, the port output must remain off unless intentionally turned on.
	PH0		General purpose input/output port.
123	SO2	D	UART2 data outpu. This function is enabled when the UART2 data output is enabled.
	PH1		General purpose input/output port. This function is enabled when the data output function of UART2 is disabled.
124	SCK2	D	UART2 clock input/output pin. This function is enabled either when the UART2 clock output is enabled or when UART2 inputs the external clock signal.
	PH2		General purpose input/output port. This function is enabled when UART2 is not using the external clock signal with the UART2 clock output function disabled.
125	SI3	D	UART3 data input. Since this input is used as required when UART3 is in input operation, the port output must remain off unless intentionally turned on.
	PH3		General purpose input/output port.
126	SO3	D	UART3 data outpu. This function is enabled when the UART3 data output is enabled.
	PH4		General purpose input/output port. This function is enabled when the data output function of UART3 is disabled.
127	SCK3	D	UART0 clock input/output pin. This function is enabled either when the UART3 clock output is enabled or when UART3 inputs the external clock signal.
	PH5		General purpose input/output port. This function is enabled when UART3 is not using the external clock signal with the UART3 clock output function disabled.
128	SI4	D	UART4 data input. Since this input is used as required when UART4 is in input operation, the port output must remain off unless intentionally turned on.
	PG0		General purpose input/output port.
129	SO4	D	UART4 data output. This function is enabled when the UART4 data output is enabled.
	PG1		General purpose input/output port. This function is enabled when the data output function of UART4 is disabled.
130	SCK4	D	UART4 clock input/output pin. This function is enabled either when the UART4 clock output is enabled or when UART4 inputs the external clock signal.
	PG2		General purpose input/output port. This function is enabled when UART4 is not using the external clock signal with the UART4 clock output function disabled.
131	SI5	D	Data input for serial I/O5. Since this input is used as required when serial I/O5 is in input operation, the port output must remain off unless intentionally turned on.
	PG3		General purpose input/output port.
132	SO5	D	Data output for serial I/O5. This function is enabled when the serial I/O5 data output is enabled.
	PG4		General purpose input/output port. This function is enabled when the I/O5 data output function is disabled.

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Pin no.	Pin name	Circuit type	Description
133	SCK5	D	Clock innput/output for serial I/O5. This function is enabled when serial I/O5 is using the external shift clock mode, or serial I/O5 clock output function is enabled.
	PG5		General purpose input/output port. This function is enabled when serial I/O5 is not using the external shift clock mode with the serial I/O5 clock output function disabled.
134	$\overline{\text{NMI}}$	H	NMI (Non Maskable Interrupt) input
135	X1A	B	Output clock cycle time. Sub clock
137	X0A	B	Input clock cycle time. Sub clock
138 to 140	MD2 to MD0	H, J	2 to 0Mode Pins. The levels applied to these pins set the basic operating mode. Connect VCC or VSS. Input circuit configuration: The production model (masked-ROM model) is type “H”. The Flash ROM model is type “J”.
141	X0	A	Input clock cycle time. Main clock
143	X1	A	Output clock cycle time. Main clock
144	$\overline{\text{INIT}}$	I	External reset input
147	DREQ2	C	External input for DMA transfer requests. Since this input is used as required when selected as a DMA start source, the port output must remain off unless intentionally turned on.
	PC0		General purpose input/output port.
148	DACK2	C	External acknowledge output for DMA transfer requests. This function is enabled when the transfer request acceptance output for DMA is enabled.
	PC1		General purpose input/output port. This function is enabled when the transfer request acceptance output for DMA is enabled.
149	DEOP2	C	Completion output for DMA external transfer. This function is enabled when the external transfer end output for DMA is enabled.
	DSTP2		Stop input for DMA external transfer. This function is enabled when the external transfer stop input for DMA is enabled.
	PC2		General purpose input/output port. This function is enabled when the external transfer end output and external transfer stop input for DMA are disabled.
150	DREQ0	C	External input for DMA transfer requests. Since this input is used as required when selected as a DMA start source, the port output must remain off unless intentionally turned on.
	PB0		General purpose input/output port.
151	DACK0	C	External acknowledge output for DMA transfer requests. This function is enabled when the transfer request acceptance output for DMA is enabled.
	PB1		General purpose input/output port. This function is enabled when the transfer request acceptance output for DMA is disabled.

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Pin no.	Pin name	Circuit type	Description
152	DEOP0	C	Completion output for DMA external transfer. This function is enabled when the external transfer end output for DMA is enabled.
	DSTP0		Stop input for DMA external transfer. This function is enabled when the external transfer stop input for DMA is enabled.
	PB2		General purpose input/output port. This function is enabled when the external transfer end output and external transfer stop input for DMA are disabled.
153	DREQ1	C	External input for DMA transfer requests. Since this input is used as required when selected as a DMA start source, the port output must remain off unless intentionally turned on.
	PB3		General purpose input/output port.
154	DACK1	C	External acknowledge output for DMA transfer requests. This function is enabled when the transfer request acceptance output for DMA is enabled.
	PB4		General purpose input/output port. This function is enabled when the external transfer request acceptance output for DMA is disabled.
155	DEOP1	C	Completion output for DMA external transfer. This function is enabled when the external transfer end output for DMA is enabled.
	DSTP1		Stop input for DMA external transfer. This function is enabled when the external transfer stop input for DMA is enabled.
	PB5		General purpose input/output port. This function is enabled when the external transfer end output and external transfer stop input for DMA are disabled.
156	$\overline{\text{IOWR}}$	C	Write strobe output for DMA fly-by transfer. This function is enabled when the DMA fly-by transfer write strobe output is enabled.
	PB6		General purpose input/output port. This function is enabled when the DMA fly-by transfer write strobe output is disabled.
157	$\overline{\text{IORD}}$	C	Read storobe output for DMA fly-by transfer. This function is enabled when the DMA fly-by transfer read strobe output is enabled.
	PB7		General purpose input/output port. This function is enabled when the DMA fly-by transfer read strobe output is disabled.
158	$\overline{\text{CS0}}$	C	Chip select 0 output. Enable at external bus mode
	PA0		General purpose input/output port. This is enabled at single chip mode.
159	$\overline{\text{CS1}}$	C	Chip select 1 output. This function is enabled when the chip select 1 output is enabled.
	PA1		General purpose input/output port. This function is enabled when the chip select 1 output is disabled.
160	$\overline{\text{CS2}}$	C	Chip select 2 output. This function is enabled when the chip select 2 output is enabled.
	PA2		General purpose input/output port. This function is enabled when the chip select 2 output is disabled.

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Pin no.	Pin name	Circuit type	Description
161	$\overline{CS3}$	C	Chip select 3 output. This function is enabled when the chip select 3 output is enabled.
	PA3		General purpose input/output port. This function is enabled when the chip select 3 output is disabled.
164	RDY	D	External ready input. The pin has this function when external ready input is enabled.
	IN0		Input capture input pin. Since this input is used as required when selected as an input capture input, the port output must remain off unless intentionally turned on.
	P80		General purpose input/output port. This function is enabled when external ready signal input is disabled.
165	$\overline{BGRNT}$	D	Acknowledge output for external bus release. Outputs “L” when the external bus is released. The pin has this function when output is enabled.
	IN1		Input capture input pin. Since this input is used as required when selected as an input capture input, the port output must remain off unless intentionally turned on.
	P81		General purpose input/output port. This function is enabled when external bus release acknowledge output is disabled.
166	BRQ	D	External bus release request input. Input “1” to request release of the external bus. The pin has this function when input is enabled.
	IN2		Input capture input pin. Since this input is used as required when selected as an input capture input, the port output must remain off unless intentionally turned on.
	P82		General purpose input/output port. The pin has this function when the external bus release request input is disabled.
167	$\overline{RD}$	D	External bus read strobe output. It is available in the external bus mode.
	P83		General purpose input/output port. This is enabled at single chip mode.
168	$\overline{WR0}$	D	External bus write strobe output. It is available in the external bus mode.
	P84		General purpose input/output port. This is enabled at single chip mode.
169	$\overline{WR1}$	D	External bus write strobe output. This function is enabled when $\overline{WR1}$ output is enabled in external bus mode.
	IN3		Input capture input pin. Since this input is used as required when selected as an input capture input, the port output must remain off unless intentionally turned on.
	P85		General purpose input/output port. The pin has this function when the external bus write-enable output is disabled.
170	SYSCLK	C	System clock output The pin has this function when system clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in stop mode.)
	P90		General purpose input/output port. The pin has this function when system clock output is disabled.
171	P91	C	General purpose input/output port.

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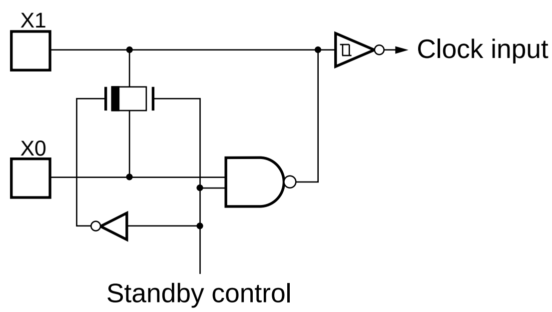
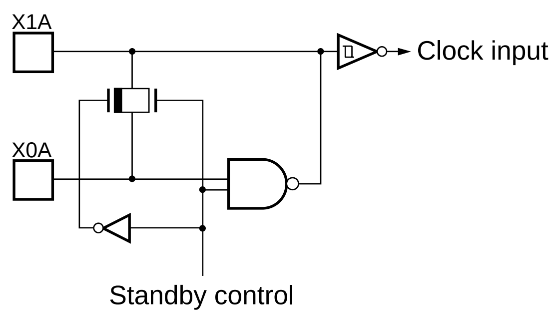
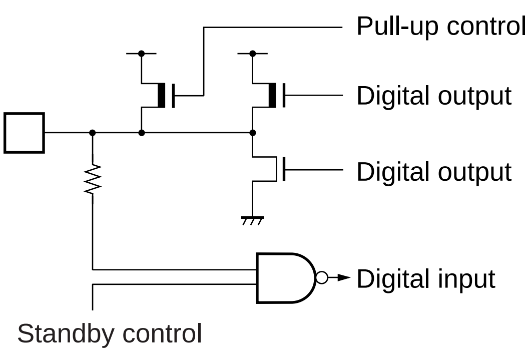
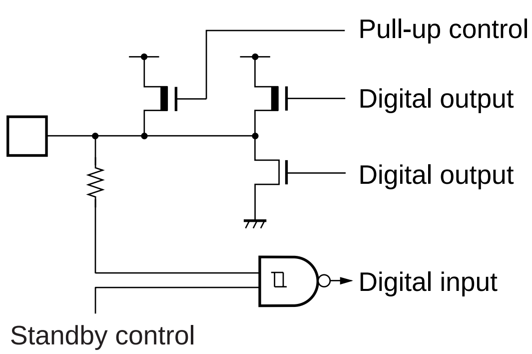
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Pin no.	Pin name	Circuit type	Description
172	MCLK	C	Memory clock output. This function is enabled when the memory clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in sleep/stop mode.)
	P92		General purpose input/output port. This function is enabled when the memory clock output is disabled.
173	P93	C	General purpose input/output port.
174	$\overline{\text{AS}}$	C	Address strobe output. This function is enabled when address strobe output is enabled.
	P94		General purpose input/output port. This function is enabled when address load output is disabled.

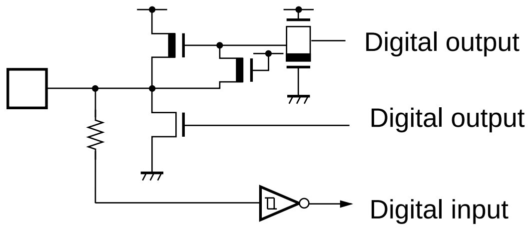
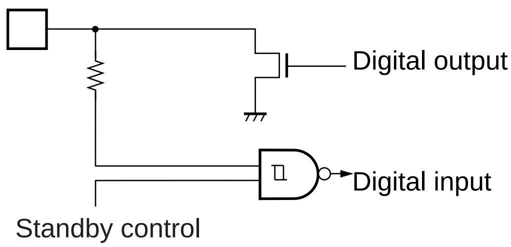
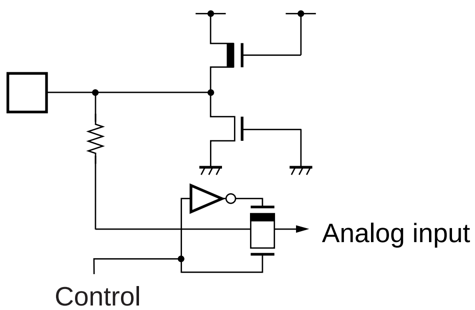
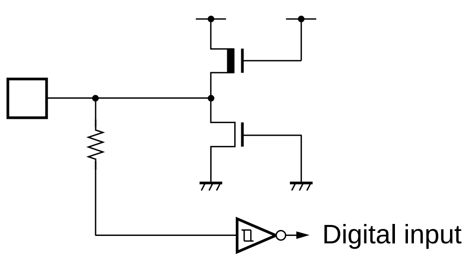
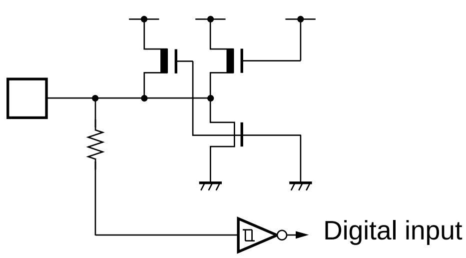
• Power supply and GND pins

Pin no.	Pin name	Description
17, 35, 65, 79, 93, 96, 114, 136, 145, 162, 175	V_{SS}	GND pins. Apply equal potential to all of the pins.
18, 36, 66, 80, 97, 115, 142, 146, 163, 176	V_{CC}	3.3 V power supply pin. Apply equal potential to all of the pins.
45	DA_{VS}	GND pin for D/A converter
46	DA_{VC}	Power supply pin for D/A converter
62	AV_{CC}	Analog power supply pin for A/D converter
63	AVRH	Reference power supply pin for A/D converter
64	AV_{SS}/AVRL	Analog GND pin for A/D converter

■ I/O CIRCUIT TYPE

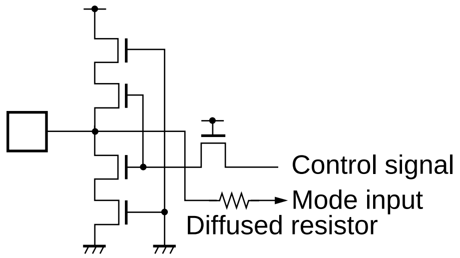
Type	Circuit type	Remarks
A		• Oscillation feedback resistance: approx. 1 MΩ
B		• Oscillation feedback resistance for low speed (subclock oscillation): approx. 7 MΩ
C		• CMOS level output • CMOS level input With standby control With Pull-up control Pull-up resistance = approx. 50 kΩ (Typ) I_{OL} = 8 mA
D		• CMOS level output • CMOS level hysteresis input With standby control With Pull-up control Pull-up resistance = approx. 50 kΩ (Typ) I_{OL} = 4 mA

(Continued)

Type	Circuit type	Remarks
E		• CMOS level output • CMOS level hysteresis input With stand voltage of 5 V I_{OL} = 4 mA
F		• Nch open drain output • CMOS level hysteresis input with standby control With stand voltage of 5 V I_{OL} = 15 mA
G		• Analog input with switch
H		• CMOS level hysteresis input
I		• CMOS level hysteresis input with pull-up resistor Pull-up resistance = approx. 50 kΩ (Typ)

(Continued)

(Continued)

Type	Circuit type	Remarks
J		• CMOS level input • Flash product only

■ HANDLING DEVICES

• Preventing Latchup

Latch-up may occur in a CMOS IC if a voltage greater than VCC or less than VSS is applied to an input or output pin or if an above-rating voltage is applied between VCC and VSS. A latchup,if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

• Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

• About power supply pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

• About Crystal oscillator circuit

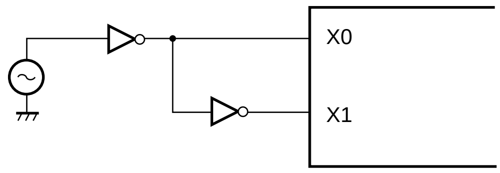
Noise near the X0, X1, X0A and X1A pins may cause the device to malfunction. Design the circuit board so that X0, X1, X0A, X1A, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0, X1, X0A and X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

• Notes on Using External Clock

When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode(oscillator stop mode) must not be used. (This is because the X1 pin stops at High level output in STOP mode.)

Using an external clock (normal)



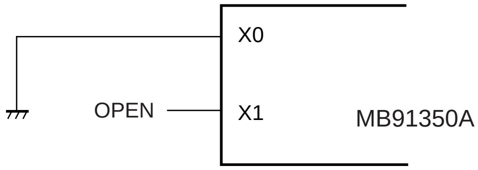
Note: STOP mode (oscillation stop mode) cannot be used.

• Clock control block

Take the oscillation stabilization wait time during Low level input to the $\overline{\text{INIT}}$ pin.

• Notes on not using the sub clock

When no oscillator is connected to the X0A and X1A pins, pull down the X0A pin and open the X1A pin.



• Treatment of NC and OPEN pins

Pins marked as NC and OPEN must be left open-circuit.

• Mode pins (MD0 to MD2)

These pins should be connected directly to V_{CC} or V_{SS}.

To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} is as short as possible and the connection impedance is low.

• Operation at start-up

The $\overline{\text{INIT}}$ pin must be at Low level when the power supply is turned on.

Immediately after the power supply is turned on, hold the Low level input to the $\overline{\text{INIT}}$ pin for the settling time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit. (For INIT via the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value.)

• About oscillation input at power on

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

• Caution on Operations during PLL Clock Mode

Even if the oscillator comes off or the clock input stops with the PLL clock selected for this microcontroller, the microcontroller may continue to operate at the free-running frequency of the PLL's internal self-oscillating oscillator circuit. Performance of this operation, however, cannot be guaranteed.

• External bus setting

This model guarantees an external bus frequency of 25 MHz.

Setting the base clock frequency to 50 MHz with DIVR1 (external bus base clock division setting register) initialized sets the external bus frequency also to 50 MHz. Before changing the base clock frequency, set the external bus frequency not exceeding 25 MHz.

• MCLK and SYSCLK

MCLK and SYSCLK has a difference that MCLK stops in SLEEP/STOP mode but SYSCLK stops only in STOP mode. Use either depending on each application.

Upon initialization, MCLK becomes invalid (PORT) and SYSCLK becomes valid. To use MCLK, set the port function register (PFR) to select the use of that clock.

• Pull-up control

Connecting a pull-up resistor to the pin serving as an external bus pin cannot a guarantee the "■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4) Normal Bus Access Read/Write Operation, (5) Multiplex Bus Access Read/Write operation and (7) Hold Timing".

Even the port for which a pull-up resistor has been set is invalid in stop mode with HIZ = 1 or in hardware standby mode.

• Sub clock select

Immediately after switching from main clock mode to subclock mode for the clock source, insert at least one NOP instruction.

```
(ldi    #0x0b, r0)
(ldi    #_CLKR, r12)
stb     r0, @r12        // sub-clock mode
nop                     // Must insert NOP instruction
```

• Bit Search Module

The BSD0, BSD1, and BDSC registers are accessed only in words.

• D-bus memory

Do not allocate the code area in memory on the D-bus because no instruction fetch takes place to the D-bus.

Executing an instruction fetch to the D-bus area causes wrong data to be interpreted as code, possibly letting the device to run out of control.

• Low Power Consumption Mode

To enter the sleep or stop mode, be sure to read the standby control register (STCR) immediately after writing to it.

Precisely, use the following sequence.

Set the I flag, ILM, and ICR to, after returning from standby mode, branch to the interrupt handler having caused the device to return.

```
(ldi    #value_of_standby, r0)
(ldi    #_STCR, r12)
stb     r0, @r12        // set STOP/SLEEP bit
ldub    @r12, r0        // Must read STCR
ldub    @r12, r0        // after reading,  go into standby
                        mode
nop                     // Must insert NOP *5
nop
nop
nop
nop
```

• Switch shared port function

To switch between the use as a port and the use as a dedicated pin, use the port function register (PFR). Note, however, that bus pins are switched depending on external bus settings.

• Pre-fetch

When accessing a prefetch-enabled little endian area, be sure to use word access (in 32-bit, word length) only.

Byte or halfword access results in wrong data read.

• I/O port access

Ports are accessed only in bytes.

• Built-in RAM

Immediately after a reset is canceled, the internal RAM allocation restricting function is still working, allowing only 4 KB to be used for data and for program execution irrespective of the on-chip RAM capacity.

• Flash memory

In programming mode, Flash memory cannot be used as an interrupt vector table. A reset is possible.

• Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

1. The following operations are performed when the instruction followed by a DIVOU/DIVOS instruction results in: (a) acceptance of a user interrupt or NMI, (b) single-stepping, or (c) a break at a data event or emulator menu.
    - The D0 and D1 flags are updated in advance.
    - An EIT handling routine (user interrupt, NMI, or emulator) is executed.
    - Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1).
2. The following operations are performed when the ORCCR/STILM/MOVRi and PS instructions are executed.
    - The PS register is updated in advance.
    - An EIT handling routine (user interrupt, NMI, or emulator) is executed.
    - Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1).

[Note on debugger]

• Step execution of RETI command

If an interrupt occurs frequently during single-stepping, the corresponding interrupt handling routine is executed repeatedly. This will prevent the main routine and low-interrupt-level programs from being executed. (Whenever RETI is single-stepped when interrupts by the timebase timer have been enabled, for example, the timebase timer routine causes a break at the beginning.)

Disable the corresponding interrupt when the corresponding interrupt handling routine no longer needs debugging.

• Break function

If the address at which to cause a hardware break (including a event break) is set to the address currently contained in the system stack pointer or in the area containing the stack pointer, the user program causes a break after execution of one instruction.

To prevent this, do not set (word) access to the area containing the address in the system stack pointer as the target of a hardware break (including an event break).

• Internal ROM area

Do not set an area of internal ROM as a DMAC transfer destination.

• Simultaneous occurrences of a software break (INTE instruction) and a user interrupt/NMI

When an INTE instruction and a user interrupt/NMI are accepted simultaneously, the emulator debugger reacts as follows.

The emulator debugger stops while indicating a location in the user program, which is not a user-specified breakpoint. (It stops with the beginning of the user interrupt/NMI handling routine indicated.)

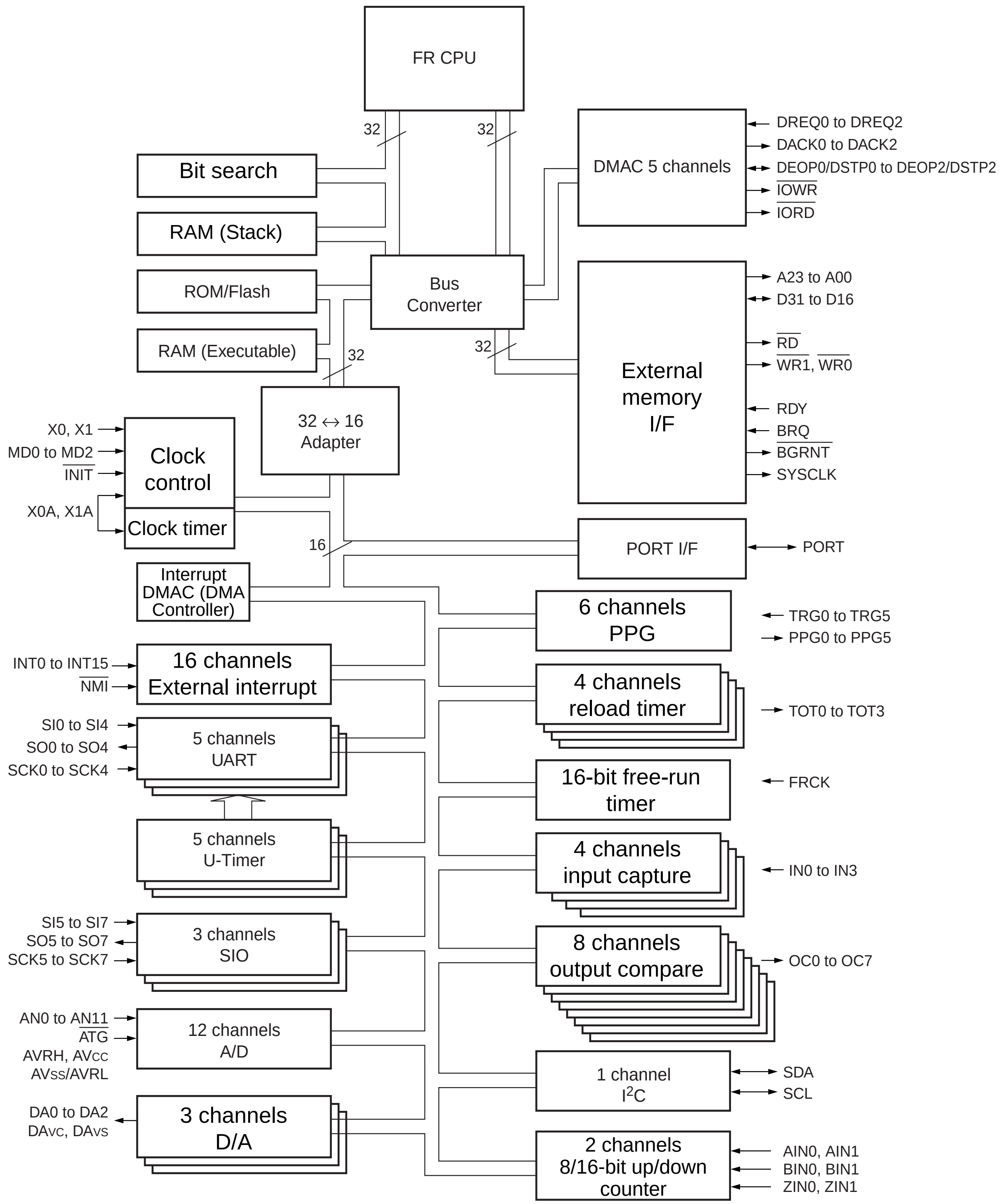
The user program cannot be re-executed correctly.

To prevent this problem, follow the instructions below.

When a software break and a user interrupt/NMI occur simultaneously, the emulator debugger may react as follows.

- The debugger stops pointing to a location other than the programmed breakpoints.
- The halted program is not re-executed correctly.
  If this symptom occurs, use a hardware break in place of a hardware break. When using a monitor debugger, do not set a break at the relevant location.
- A stack pointer placed in an area set for a DSU operand break can cause a malfunction. Do not apply a data event break to access to the area containing the address of a system stack pointer.

■ BLOCK DIAGRAM



	MB91F355A	MB91F356B	MB91355A	MB91354A
ROM/Flash	512 KB (Flash)	256 KB (Flash)	512 KB	384 KB
RAM (Stack)	16 KB	16 KB	16 KB	16 KB
RAM (Executable)	8 KB	8 KB	8 KB	8 KB

■ CPU AND CONTROL UNIT

Internal architecture

The FR family CPU is a high performance core based on a RISC architecture while incorporating advanced instructions for embedded controller applications.

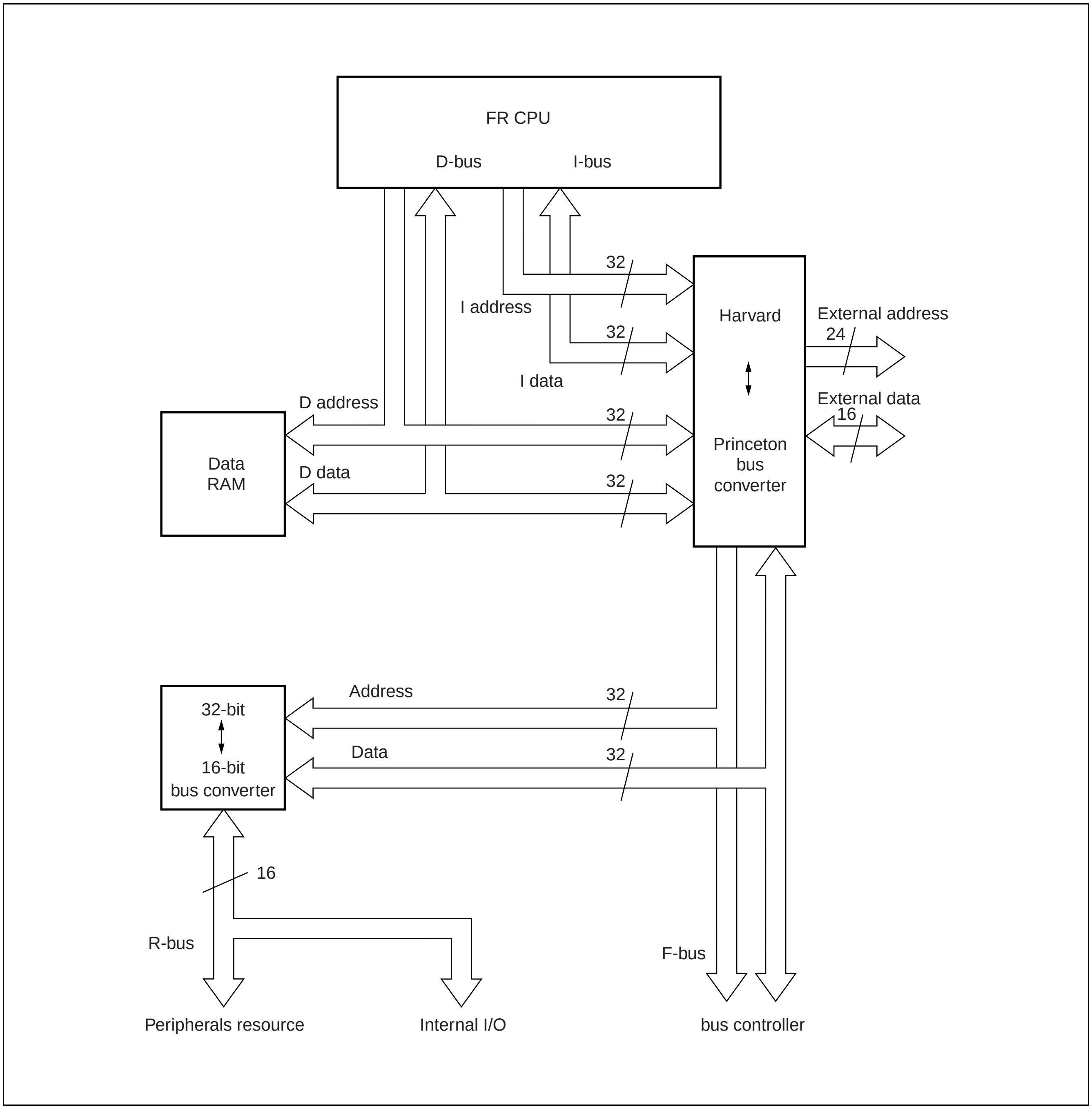
1. Features

- RISC architecture employed. Basic instructions: Executed at 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4GB linear memory space
- Multiplier integrated.
  32-bit x 32-bit multiplication: 5 cycles.
  16-bit x 16-bit multiplication: 3 cycles
- Enhanced interrupt servicing.
  Fast response speed (6 cycles).
  Multiple interrupts supported.
  Level masking (16 levels)
- Enhanced I/O manipulation instructions.
  Memory-to-memory transfer instructions, Bit manipulation instructions
- High code efficiency. Basic instruction word length: 16-bit
- Low-power consumption. Sleep mode and stop mode
- Gear function

2. Internal architecture

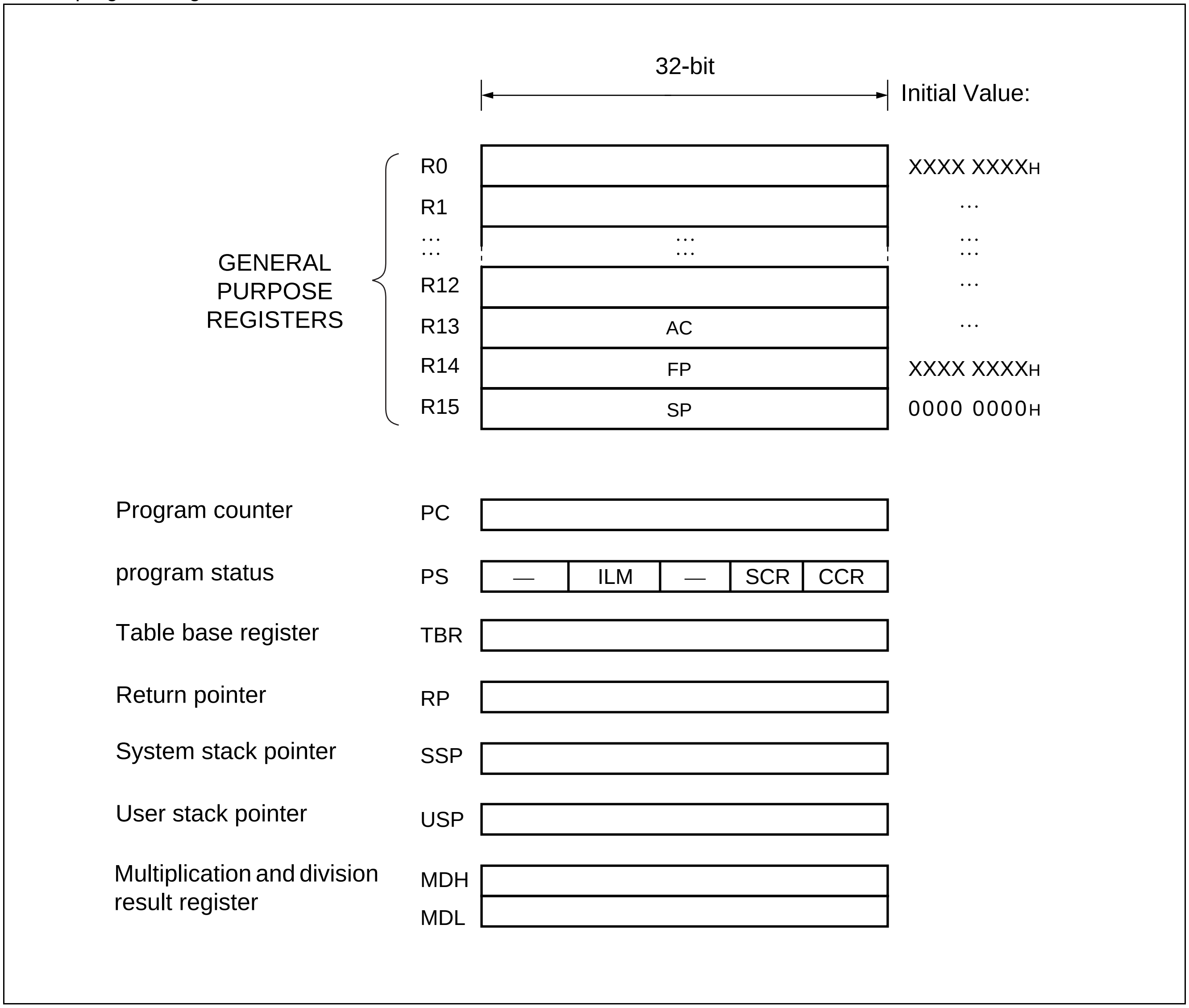
The FR-family CPU has a Harvard architecture in which the instruction and data buses are separated.

The 32-bit/16-bit bus converter is connected to a 32-bit bus (F-bus), providing an interface between the CPU and peripheral resources. The Harvard-Princeton bus converter is connected to both of the I-bus and D-bus, providing an interface between the CPU and the bus controller.



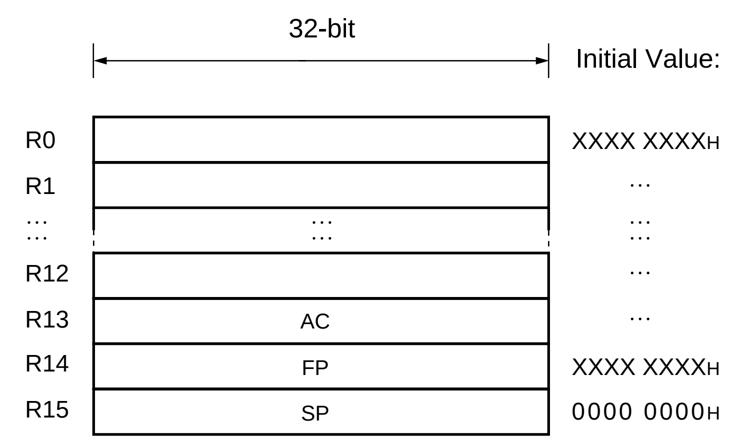
3. Programming model

• Basic programming model



4. Register

General purpose registers



Registers R0 to R15 are general-purpose registers. The registers are used as the accumulator and memory access pointers for CPU operations.

Of these 16 registers, the registers listed below are intended for special applications, for which some instructions are enhanced.

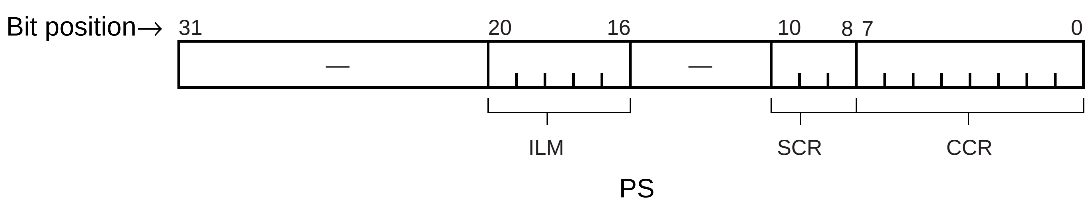
R13 : Virtual accumulator
R14 : frame pointer
R15 : Stack pointer

The initial values of R0 to R14 after a reset are indeterminate. R15 is initialized to 0000 0000_H (SSP value).

• PS (Program Status)

This register holds the program status and is divided into the ILM, SCR, and CCR.

The undefined bits in the following illustration are all reserved bits. Reading these bits always returns “0”. Writing to them has no effect.



• CCR (Condition Code Register)

7	6	5	4	3	2	1	0
—	—	S	I	N	Z	V	C

CCR

Initial Value:
- - $00XXXX_B$

S : Stack flag. Cleared to “0” by a reset.
I : Interrupt enable flag. Cleared to “0” by a reset.
N : Negative flag. The initial value after a reset is indeterminate.
Z : Zero flag. The initial value after a reset is indeterminate.
V : Overflow flag. The initial value after a reset is indeterminate.
C : Carry flag. The initial value after a reset is indeterminate.

• SCR (System Condition code Register)

10	9	8
D1	D0	T

SCR

Initial Value:
$XX0_B$

Flag for step dividing
Stores intermediate data for stepwise multiplication operations.
Step trace trap flag
A flag specifying whether the step trace trap function is enabled or not.
Emulator use step trace trap function. The function cannot be used by the user program when using the emulator.

• ILM

20	19	18	17	16
ILM4	ILM3	ILM2	ILM1	ILM0

ILM

Initial Value:
01111_B

This register stores the interrupt level mask value. The value in the ILM register is used as the level mask.
Initialized to “15” (01111_B) by a reset.

• PC (Program Counter)

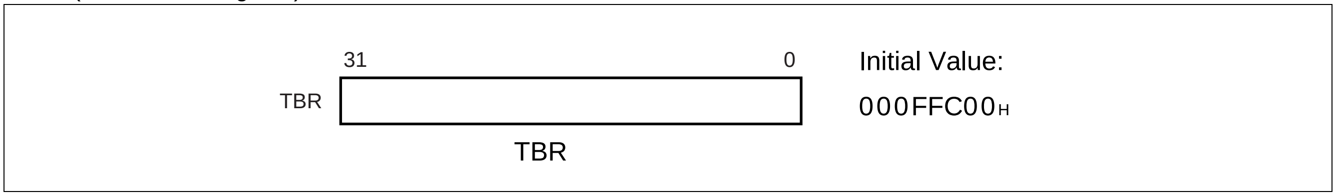
	31 … 0
PC	

PC

Initial Value:
XXXXXXXX_H

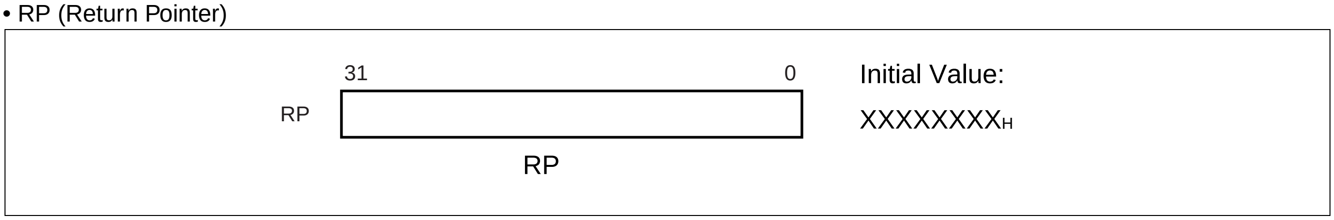
The program counter contains the address of the instruction currently being executed.
The initial value after a reset is indeterminate.

• TBR (Table Base Register)



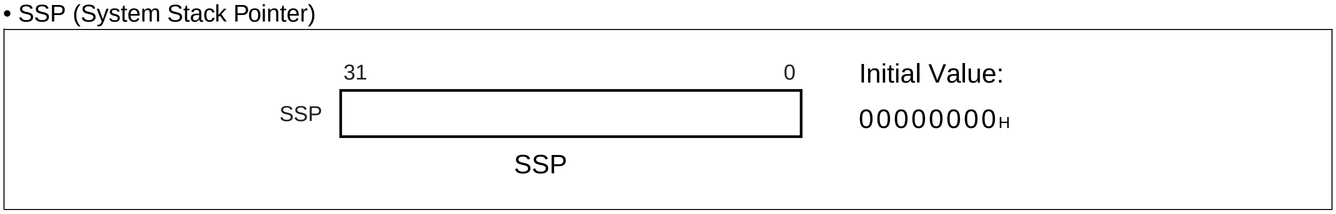
The table base register contains the start address of the vector table used for servicing EIT events.
The initial value after a reset is 000FFC00$_H$

• RP (Return Pointer)



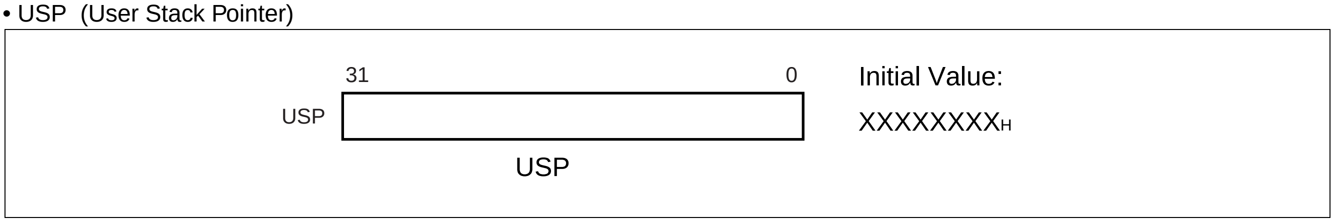
The return pointer contains the address to which to return from a subroutine.
When the CALL instruction is executed, the value in the PC is transferred to the RP.
When the RET instruction is executed, the value in the RP is transferred to the PC.
The initial value after a reset is indeterminate.

• SSP (System Stack Pointer)



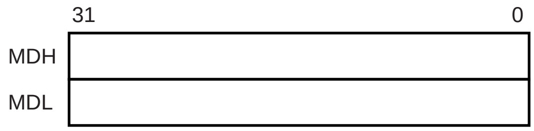
The SSP is the system stack pointer and functions as R15 when the S flag is “0”.
The SSP can be explicitly specified.
The SSP is also used as the stack pointer that specifies the stack for saving the PS and PC when an EIT event occurs.
The initial value after a reset is 00000000$_H$

• USP (User Stack Pointer)



The USP is the user stack pointer and functions as R15 when the S flag is “1”.
The SSP can be explicitly specified.
The initial value after a reset is indeterminate.
This pointer cannot be used by the RETI instruction.

• Multiply & Divide registers



Multiplication and division result register

These registers hold the results of a multiplication or division. Each of them is 32-bit long.
The initial value after a reset is indeterminate.

■ MODE SETTINGS

The FR family uses mode pins (MD2 to MD0) and a mode register (MODR) to set the operation mode.

1. Mode Pins

The MD2, MD1, and MD0 pins specify how the mode vector fetch is performed.

Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	The bus width is specified by the mode register.

Values other than those listed in the table are prohibited.

2. Mode Register (MODR)

The data written to the mode register at 000F FFF8$_H$ using mode vector fetch is called mode data.

After an operation mode has been set in the mode register (MODR), the device operates in the operation mode.

The mode register is set by any reset source. User programs cannot write data to the mode register.

Note : Conventionally the FR family has nothing at addresses (0000 07FF$_H$) in the mode register.

<Register description>

MODR	7	6	5	4	3	2	1	0	Initial Value
000F FFF8$_H$	0	0	0	0	0	ROMA	WTH1	WTH0	XXXXXXXX$_B$

Bits 2 to 0 (ROMA, WTH1, WTH0): Operation mode setting bits

[bit 7 to bit 3] Reserved bit

Be sure to set this bit to “00000”. Operation is not guaranteed when any value other than “00000” is set.

[bit 2] ROMA (internal ROM enable bit)

The ROMA bit is used to set whether to enable the internal F-bus RAM and F-bus ROM areas.

ROMA	function	Remarks
0	External ROM mode	Internal F-bus RAM is valid; the area (80000$_H$ to 100000$_H$) of internal ROM is used as an external area.
1	Internal ROM mode	Internal F-bus RAM and F-bus ROM become valid.

[bit 1, bit 0] WTH1, WTH0 (Bus width setting bits)

Used to set the bus width to be used in external bus mode.

When the operation mode is the external bus mode, this value is set in bits BW1 and BW0 in AMD0 (CS0 area).

WTH1	WTH0	function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	
1	0	—	Setting disabled
1	1	single chip mode	single chip mode

■ MEMORY SPACE

1. Memory space

The FR family has 4 GB of logical address space (2^{32} addresses) available to the CPU by linear access.

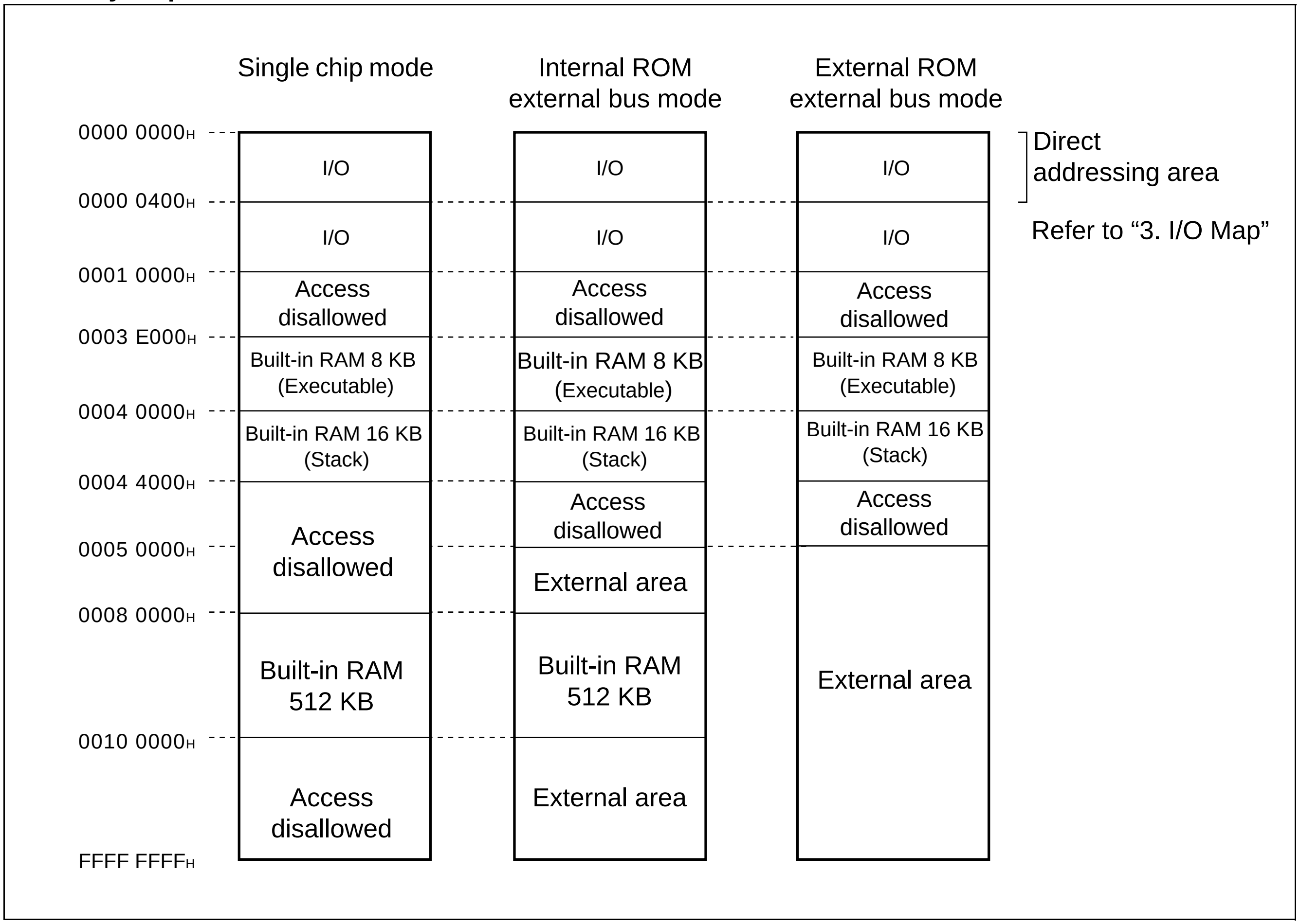
• Direct Addressing Areas

The following address space areas are used as I/O areas.
These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.
The size of directly addressable areas depends on the length of the data being accessed as shown below.

→ byte data access : 000_H to $0FF_H$
→ half word data access : 000_H to $1FF_H$
→ word data access : 000_H to $3FF_H$

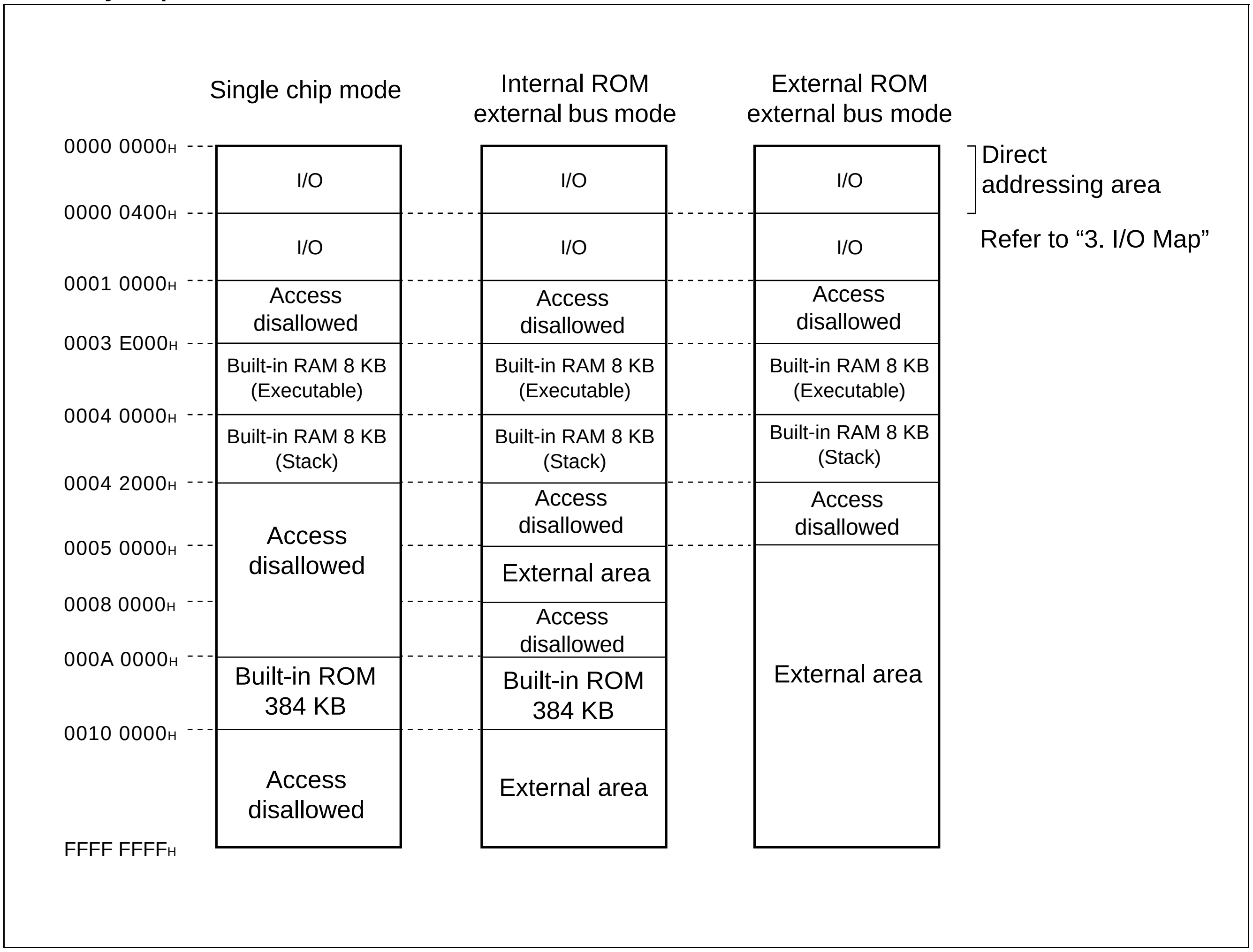
2. Memory Map

• Memory map of MB91F355A/MB91355A



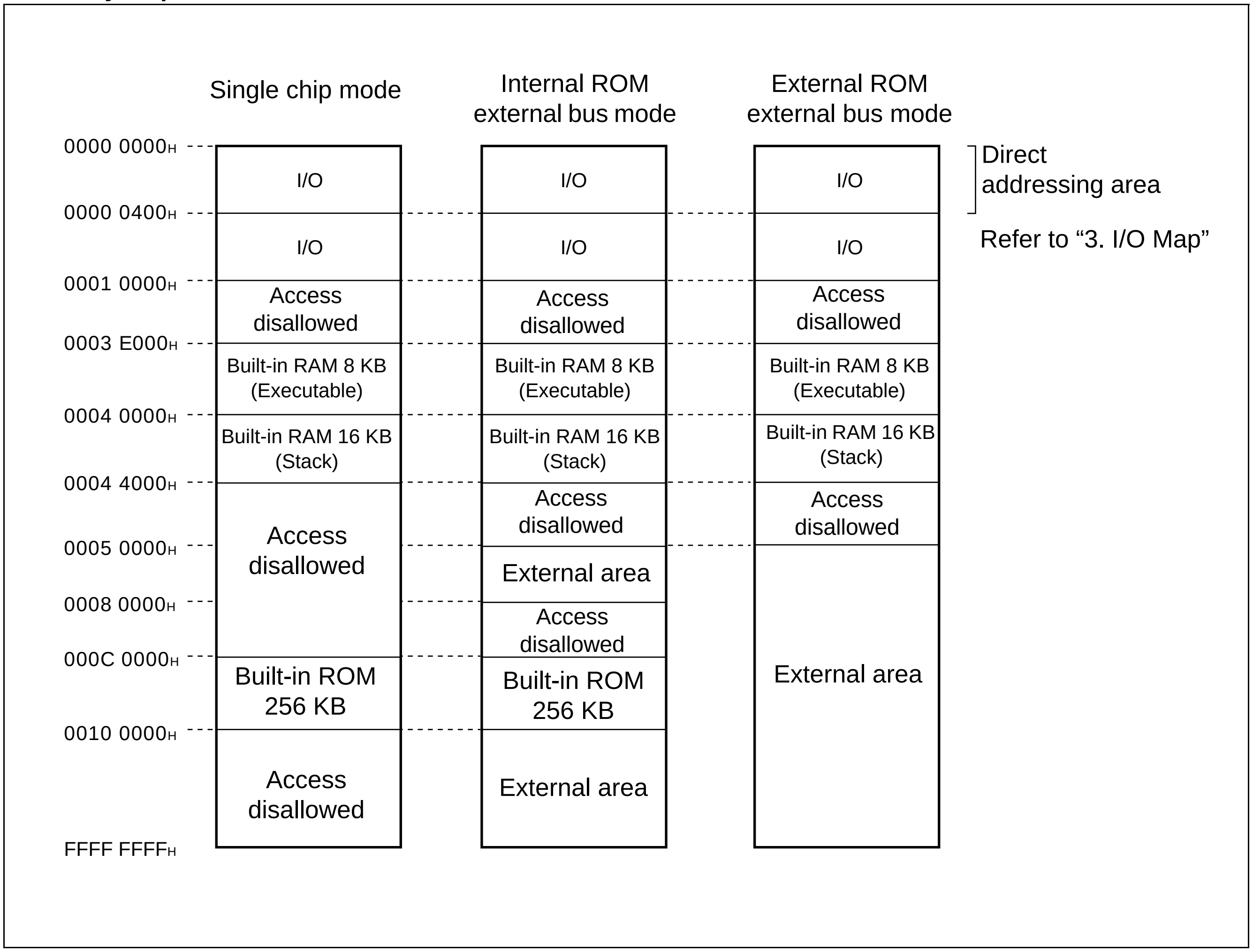
- Each mode is set depending on the mode vector fetch after $\overline{INIT}$ is negated.
- The MB91V350A uses the area of 512 KB of internal ROM as emulation RAM in the MB91355A memory map. The internal RAM (Instruction) has been expanded from 8 KB to 16 KB.
- The available area of internal RAM is restricted immediately after a reset is canceled. When the setting of the available area is updated, the instruction must be followed by at least 1 NOP instruction.

● **Memory Map of MB91354A**



- Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated.
- The available area of internal RAM is restricted immediately after a reset is canceled. When the setting of the available area is updated, the instruction must be followed by at least 1 NOP instruction.

- **Memory Map of MB91356B**



- Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated.
- The available area of internal RAM is restricted immediately after a reset is canceled. When the setting of the available area is updated, the instruction must be followed by at least 1 NOP instruction.

3. I/O Map

This shows the location of the various peripheral resource registers in the memory space.

(How to read the table)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	T-unit Port Data Register

- Read/write attribute, Access unit
  (B : Byte, H : Half Word, W : Word)
- Initial value after a reset
- Register name (First-column register at address 4n, second-column register at address 4n + 2)
- Location of left-most register (When using word access, the register in column 1 is in the MSB side of the data.)

Note : Initial values of register bits are represented as follows :

“1” : Initial value is “1”.
“0” : Initial Value: “0”.
“X” : Initial value is “X”.
“–” : No physical register at this location

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
000000H	—	—	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	T-unit Port Data Register
000004H	PDR4 [R/W] B XXXXXXXX	PDR5 [R/W] B XXXXXXXX	PDR6 [R/W] B XXXXXXXX	—	
000008H	PDR8 [R/W] B - - XXXXXX	PDR9 [R/W] B - - - XXXXX	PDRA [R/W] B - - - - XXXX	PDRB [R/W] B XXXXXXXX	
00000CH	PDRC [R/W] B - - - - - XXX	—			
000010H	PDRG[R/W] B - - XXXXXX	PDRH [R/W] B - - XXXXXX	PDRI [R/W] B - - XXXXXX	PDRJ [R/W] B XXXXXXXX	R-bus Port Data Register
000014H	PDRK [R/W] B XXXXXXXX	PDRL [R/W] B - - - - - - XX	PDRM [R/W] B - - XXXXXX	PDRN [R/W] B - - XXXXXX	
000018H	PDRO [R/W] B XXXXXXXX	PDRP [R/W] B - - - - XXXX	—	—	
00001CH	—				
000020H	—	—	—	—	Reserved
000024H	SMCS5 [R/W] B, H*3 00000010 - - - - 00 - -		SES5 [R/W] B*3 - - - - - - 00	SDR5 [R/W] B*3 XXXXXXXX	SIO 5*3

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block diagram
000028H	SMCS6 [R/W] B, H 00000010 - - - - 00 - -		SES6 [R/W] B - - - - - - 00	SDR6 [R/W] B XXXXXXXX	SIO 6
00002CH	SMCS7 [R/W] B, H 00000010 - - - - 00 - -		SES7 [R/W] B - - - - - - 00	SDR7 [R/W] B XXXXXXXX	SIO 7
000030H	—	—	CDCR5 [R/W] B 0---1111	—*1	SIO Prescaler 5
000034H	CDCR6 [R/W] B 0 - - - 1111	—*1	CDCR7 [R/W] B 0 - - - 1111	—*1	SIO Prescaler 6, 7
000038H	—	SRCL5 [W] B - - - - - - - -	SRCL6 [W] B - - - - - - - -	SRCL7 [W] B - - - - - - - -	SIO5 to SIO7
00003CH	—	—	—	—	Reserved
000040H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000		Ext int (INT0 to INT7)
000044H	DICR [R/W] B, H, W - - - - - - - 0	HRCL [R/W] B, H, W 0 - - 11111	—		DLYI/I-unit
000048H	TMRLR [W] H, W XXXXXXXX XXXXXXXX		TMR [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR [R/W] B, H, W - - - - 0000 00000000		
000050H	TMRLR [W] H, W XXXXXXXX XXXXXXXX		TMR [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR [R/W] B, H, W - - - - 0000 00000000		
000058H	TMRLR [W] H, W XXXXXXXX XXXXXXXX		TMR [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR [R/W] B, H, W - - - - 0000 00000000		
000060H	SSR [R/W] B, H, W 00001000	SIDR/SODR [R/W] B, H, W XXXXXXXX	SCR [R/W] B, H, W 00000100	SMR [R/W] B, H, W 00 - - 0 - - -	UART0
000064H	UTIM [R] H (UTIMR [W] H) 00000000 00000000		DRCL [W] B - - - - - - - -	UTIMC [R/W] B 0 - - 00001	U-Timer/ UART 0
000068H	SSR [R/W] B, H, W 00001000	SIDR/SODR [R/W] B, H, W XXXXXXXX	SCR [R/W] B, H, W 00000100	SMR [R/W] B, H, W 00 - - 0 - - -	UART1
00006CH	UTIM [R] H (UTIMR [W] H) 00000000 00000000		DRCL [W] B - - - - - - - -	UTIMC [R/W] B 0 - - 00001	U-Timer/ UART 1
000070H	SSR [R/W] B, H, W 00001000	SIDR/SODR [R/W] B, H, W XXXXXXXX	SCR [R/W] B, H, W 00000100	SMR [R/W] B, H, W 00 - - 0 - - -	UART2
000074H	UTIM [R] H (UTIMR [W] H) 00000000 00000000		DRCL [W] B - - - - - - - -	UTIMC [R/W] B 0 - - 00001	U-Timer/ UART 2

(Continued)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
000078H	ADCS2 [R/W]B, H, W X000XX00	ADCS1 [R/W]B, H, W 000X0000	ADCT [R/W] H, W XXXXXXXX_XXXXXXXX		A/D converter: Successive approxima-tion
00007CH	ADTH0 [R] B, H, W XXXXXXXX	ADTL0 [R] B, H, W 000000XX	ADTH1 [R] B, H, W XXXXXXXX	ADTL1 [R] B, H, W 000000XX	
000080H	ADTH2 [R] B, H, W XXXXXXXX	ADTL2 [R] B, H, W 000000XX	ADTH3 [R] B, H, W XXXXXXXX	ADTL3 [R] B, H, W 000000XX	
000084H	—	DACR2 [R/W] B, H, W - - - - - - - 0	DACR1 [R/W] B, H, W - - - - - - - 0	DACR0 [R/W] B, H, W - - - - - - - 0	D/A Converter
000088H	—	DADR2 [R/W] B, H, W XXXXXXXX	DADR1 [R/W] B, H, W XXXXXXXX	DADR0 [R/W] B, H, W XXXXXXXX	
00008CH	—	—	—	—	Reserved
000090H	—	—	—	—*1	Reserved
000094H	IBCR [R/W] B, H, W 00000000	IBSR [R] B, H, W 00000000	ITBA [R/W] B, H, W - - - - - - 00 00000000		I²C interface
000098H	ITMK [R/W] B, H, W 00 - - - - 11 11111111		ISMK [R/W] B, H, W 01111111	ISBA [R/W] B, H, W - 0000000	
00009CH	—	IDAR [R/W] B, H, W 00000000	ICCR [R/W] B, H, W 0 - 011111	IDBL [R/W] B, H, W - - - - - - - 0	
0000A0H	—	—*1	—	—*1	Reserved
0000A4H	—	—*1	—*1	—*1	
0000A8H	TMRLR [W] H, W XXXXXXXX XXXXXXXX		TMR [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 3
0000ACH	—		TMCSR [R/W] B, H, W - - - - 0000 00000000		
0000B0H	RCR1 [W] B, H, W 00000000	RCR0 [W] B, H, W 00000000	UDCR1 [R] B, H, W 00000000	UDCR0 [R] B, H, W 00000000	8/16-bit Up/Down Counter 0, 1
0000B4H	CCRH0 [R/W] B, H, W 00001000	CCRL0 [R/W] B, H, W 00001000	—	CSR0 [R/W] B, H, W 00000000	
0000B8H	CCRH1 [R/W] B, H, W 00001000	CCRL1 [R/W] B, H, W 00001000	—	CSR1 [R/W] B, H, W 00000000	
0000BCH	—	—	—	—	Reserved
0000C0H	SSR [R/W] B, H, W 00001000	SIDR/SODR [R/W] B, H, W XXXXXXXX	SCR [R/W] B, H, W 00000100	SMR [R/W] B, H, W 00 - - 0 - - -	UART3
0000C4H	UTIM [R] H (UTIMR [W] H) 00000000 00000000		—	UTIMC [R/W] B 0 - - 00001	U-Timer/ UART 3
0000C8H	SSR [R/W] B, H, W 00001000	SIDR/SODR [R/W] B, H, W XXXXXXXX	SCR [R/W] B, H, W 00000100	SMR [R/W] B, H, W 00 - - 0 - - -	UART4

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block diagram
0000CC$_H$	UTIM [R] H (UTIMR [W] H) 00000000 00000000		—	UTIMC [R/W] B 0 - - 00001	U-Timer/ UART 4
0000D0$_H$	EIRR1 [R/W] B, H, W 00000000	ENIR1 [R/W]B, H, W 00000000	ELVR1 [R/W] B, H, W 00000000		Ext int (INT8-15)
0000D4$_H$	TCDT [R/W] H, W 00000000 00000000		—	TCCS [R/W] B, H, W 00000000	16-bit Free run Timer
0000D8$_H$	IPCP1 [R] H, W XXXXXXXX XXXXXXXX		IPCP0 [R] H, W XXXXXXXX XXXXXXXX		16-bit ICU
0000DC$_H$	IPCP3 [R] H, W XXXXXXXX XXXXXXXX		IPCP2 [R] H, W XXXXXXXX XXXXXXXX		
0000E0$_H$	—	ICS23 [R/W] B, H, W 00000000	—	ICS01 [R/W] B, H, W 00000000	
0000E4$_H$	OCCP1 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP0 [R/W] H, W XXXXXXXX XXXXXXXX		16-bit OCU *3
0000E8$_H$	OCCP3 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP2 [R/W] H, W XXXXXXXX XXXXXXXX		
0000EC$_H$	OCCP5 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP4 [R/W] H, W XXXXXXXX XXXXXXXX		
0000F0$_H$	OCCP7 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP6 [R/W] H, W XXXXXXXX XXXXXXXX		
0000F4$_H$	OCS23 [R/W] B, H, W 1110110 00001100		OCS01 [R/W] B, H, W 1110110 00001100		
0000F8$_H$	OCS67 [R/W] B, H, W 1110110 00001100		OCS45 [R/W] B, H, W 1110110 00001100		
0000FC$_H$	—	—	—	—	Reserved
000100$_H$ to 000114$_H$	—	—	—	—	Reserved
000118$_H$	GCN10 [R/W] H 00110010_00010000		—	GCN20 [R/W] B 00000000	PPG Control 0
00011C$_H$	—		—		Reserved
000120$_H$	PTMR0 [R] H, W 11111111_11111111		PCSR0 [W] H, W XXXXXXXX_XXXXXXXX		PPG0
000124$_H$	PDUT0 [W] H, W XXXXXXXX_XXXXXXXX		PCNH0 [R/W] B, H, W 00000000	PCNL0 [R/W] B, H, W 00000000	
000128$_H$	PTMR1 [R] H, W 11111111_11111111		PCSR1 [W] H, W XXXXXXXX_XXXXXXXX		PPG1
00012C$_H$	PDUT1 [W] H, W XXXXXXXX_XXXXXXXX		PCNH1 [R/W] B, H, W 00000000	PCNL1 [R/W] B, H, W 00000000	

(Continued)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
000130_H	PTMR2 [R] H, W 11111111_11111111		PCSR2 [W] H, W XXXXXXXX_XXXXXXXX		PPG2
000134_H	PDUT2 [W] H, W XXXXXXXX_XXXXXXXX		PCNH2 [R/W] B, H, W 00000000	PCNL2 [R/W] B, H, W 00000000	
000138_H	PTMR3 [R] H, W 11111111_11111111		PCSR3 [W] H, W XXXXXXXX_XXXXXXXX		PPG3
$00013C_H$	PDUT3 [W] H, W XXXXXXXX_XXXXXXXX		PCNH3 [R/W] B, H, W 00000000	PCNL3[R/W] B, H, W 00000000	
000140_H	PTMR4 [R] H, W 11111111_11111111		PCSR4 [W] H, W XXXXXXXX_XXXXXXXX		PPG4
000144_H	PDUT4 [W] H, W XXXXXXXX_XXXXXXXX		PCNH4 [R/W] B, H, W 00000000	PCNL4 [R/W] B, H, W 00000000	
000148_H	PTMR5 [R] H, W 11111111_11111111		PCSR5 [W] H, W XXXXXXXX_XXXXXXXX		PPG5
$00014C_H$	PDUT5 [W] H, W XXXXXXXX_XXXXXXXX		PCNH5 [R/W] B, H, W 00000000	PCNL5 [R/W] B, H, W 00000000	
000150_H to $0001FC_H$	—				Reserved
000200_H	DMACA0 [R/W] B, H, W*2 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] B, H, W*2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] B, H, W*2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] B, H, W*2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] B, H, W*2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H	—				

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block diagram
00022CH to 00023CH	—				Reserved
000240H	DMACR [R/W] B 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 00027CH	—				Reserved
000280H	FRLR [R/W] B, H, W - - - - - - 01*3	—	—	—	F-bus RAM capacity limit
000284H to 00038CH	—				Reserved
000390H	DRLR [R/W] B, H, W - - - - - - 01*3	—	—	—	D-bus RAM capacity limit
000394H to 0003ECH	—				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDRG[R/W] B - - 000000	DDRH [R/W] B - - 000000	DDRI [R/W] B - - 000000	DDRJ [R/W] B 00000000	R-bus Data Direction Register
000404H	DDRK [R/W] B 00000000	DDRL [R/W] B - - - - - - 00	DDRM [R/W] B - - 000000	DDRN [R/W] B - - 000000	
000408H	DDRO [R/W] B 00000000	DDRP [R/W] B - - - - 0000	—		
00040CH	—				
000410H	PFRG [R/W] B - - 00 - 00 -	PFRH [R/W] B - - 00 - 00 -	PFRI [R/W] B - - 00 - 00 -	—	R-bus Port Function Register
000414H	————	PFRL [R/W] B - - - - - - 00	PFRM [R/W] B - - 00 - 00 -	PFRN [R/W] B - - 000000	
000418H	PFRO [R/W] B 00000000	PFRP [R/W] B - - - - 0000	—		
00041CH	—				Reserved

(Continued)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
000420H	PCRG [R/W] B - - 000000	PCRH [R/W] B - - 000000	PCRI [R/W] B - - 000000	—	R-bus Pull-up Control Register
000424H	—	—	PCRM [R/W] B - - 000000	PCRN [R/W] B - - 000000	
000428H	PCRO [R/W] B 00000000	PCRP [R/W] B - - - - 0000	—	—	
00042CH to 00043CH	—				Reserved
000440H	ICR00 [R/W] B, H, W - - - 11111	ICR01 [R/W] B, H, W - - - 11111	ICR02 [R/W] B, H, W - - - 11111	ICR03 [R/W] B, H, W - - - 11111	Interrupt Control unit
000444H	ICR04 [R/W] B, H, W - - - 11111	ICR05 [R/W] B, H, W - - - 11111	ICR06 [R/W] B, H, W - - - 11111	ICR07 [R/W] B, H, W - - - 11111	
000448H	ICR08 [R/W] B, H, W - - - 11111	ICR09 [R/W] B, H, W - - - 11111	ICR10 [R/W] B, H, W - - - 11111	ICR11 [R/W] B, H, W - - - 11111	
00044CH	ICR12 [R/W] B, H, W - - - 11111	ICR13 [R/W] B, H, W - - - 11111	ICR14 [R/W] B, H, W - - - 11111	ICR15 [R/W] B, H, W - - - 11111	
000450H	ICR16 [R/W] B, H, W - - - 11111	ICR17 [R/W] B, H, W - - - 11111	ICR18 [R/W] B, H, W - - - 11111	ICR19 [R/W] B, H, W - - - 11111	
000454H	ICR20 [R/W] B, H, W - - - 11111	ICR21 [R/W] B, H, W - - - 11111	ICR22 [R/W] B, H, W - - - 11111	ICR23 [R/W] B, H, W - - - 11111	
000458H	ICR24 [R/W] B, H, W - - - 11111	ICR25 [R/W] B, H, W - - - 11111	ICR26 [R/W] B, H, W - - - 11111	ICR27 [R/W] B, H, W - - - 11111	
00045CH	ICR28 [R/W] B, H, W - - - 11111	ICR29 [R/W] B, H, W - - - 11111	ICR30 [R/W] B, H, W - - - 11111	ICR31 [R/W] B, H, W - - - 11111	
000460H	ICR32 [R/W] B, H, W - - - 11111	ICR33 [R/W] B, H, W - - - 11111	ICR34 [R/W] B, H, W - - - 11111	ICR35 [R/W] B, H, W - - - 11111	
000464H	ICR36 [R/W] B, H, W - - - 11111	ICR37 [R/W] B, H, W - - - 11111	ICR38 [R/W] B, H, W - - - 11111	ICR39 [R/W] B, H, W - - - 11111	
000468H	ICR40 [R/W] B, H, W - - - 11111	ICR41 [R/W] B, H, W - - - 11111	ICR42 [R/W] B, H, W - - - 11111	ICR43 [R/W] B, H, W - - - 11111	
00046CH	ICR44 [R/W] B, H, W - - - 11111	ICR45 [R/W] B, H, W - - - 11111	ICR46 [R/W] B, H, W - - - 11111	ICR47 [R/W] B, H, W - - - 11111	
000470H to 00047CH	—				
000480H	RSRR [R/W] B, H, W 10000000	STCR [R/W] B, H, W 00110011	TBCR [R/W] B, H, W 00XXXX00	CTBR [W] B, H, W XXXXXXXX	Clock Control unit
000484H	CLKR [R/W] B, H, W 00000000	WPR [W] B, H, W XXXXXXXX	DIVR0 [R/W] B, H, W 00000011	DIVR1 [R/W] B, H, W 00000000	
000488H	—	—	OSCCR [R/W] B XXXXXXX0	—	

(Continued)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
00048C$_H$	WPCR [R/W] B 00 - - - 000	—	—	—	Clock timer
000490$_H$	OSCR [R/W] B 000 - - XX0	—	—	—	Main oscillation stabilization timer
000494$_H$	RSTOP0 [W] B 00000000	RSTOP1 [W] B 00000000	RSTOP2 [W] B 00000000	RSTOP3 [W] B - - - - - 000	Peripheral stop control
000498$_H$	—	—	—	—	Reserved
00049C$_H$ to 0005FC$_H$	—				Reserved
000600$_H$	—	—	DDR2 [R/W] B 00000000	DDR3 [R/W] B 00000000	T-unit Data Direction Register
000604$_H$	DDR4 [R/W] B 00000000	DDR5 [R/W] B 00000000	DDR6 [R/W] B 00000000	—	
000608$_H$	DDR8 [R/W] B - - 000000	DDR9 [R/W] B - - - 00000	DDRA [R/W] B - - - - 0000	DDRB [R/W] B 00000000	
00060C$_H$	DDRC [R/W] B - - - - - 000	—			
000610$_H$	—	—	—	—	T-unit Port Function Register
000614$_H$	—	—	PFR6 [R/W] B 11111111	—	
000618$_H$	PFR8 [R/W] B - - 1 - - 0 - -	PFR9 [R/W] B - - - 010 - 1	PFRA [R/W] B - - - - 1111	PFRB1 [R/W] B 00000000	
00061C$_H$	PFRB2 [R/W] B 00 - - - - 00	PFRC [R/W] B - - - 00000	—	—	
000620$_H$	—	—	PCR2 [R/W] B 00000000	PCR3 [R/W] B 00000000	T-unit Pull-up Control Register
000624$_H$	PCR4 [R/W] B 00000000	PCR5 [R/W] B 00000000	PCR6 [R/W] B 00000000	—	
000628$_H$	PCR8 [R/W] B --000000	PCR9 [R/W] B 00000000	PCRA [R/W] B 00000000	PCRB [R/W] B 00000000	
00062C$_H$	PCRC [R/W] B -----000	—	—	—	
000630$_H$ to 00063C$_H$	—				Reserved
000640$_H$	ASR0 [R/W] H, W 00000000 00000000		ACR0 [R/W] B, H, W 1111XX00 00000000		T-unit
000644$_H$	ASR1 [R/W] H, W 00000000 00000000		ACR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000648$_H$	ASR2 [R/W] H, W 00000000 00000000		ACR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
00064C$_H$	ASR3 [R/W] H, W 00000000 00000000		ACR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000650$_H$	ASR4 [R/W] H, W 00000000 00000000		ACR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000654$_H$	ASR5 [R/W] H, W 00000000 00000000		ACR5 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000658$_H$	ASR6 [R/W] H, W 00000000 00000000		ACR6 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00065C$_H$	ASR7 [R/W] H, W 00000000 00000000		ACR7 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000660$_H$	AWR0 [R/W] B, H, W 01111111 11111111		AWR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000664$_H$	AWR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		T-unit
000668$_H$	AWR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR5 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00066C$_H$	AWR6 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR7 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000670$_H$	—				
000674$_H$	—				
000678$_H$	IOWR0 [R/W] B, H, W XXXXXXXX	IOWR1 [R/W] B, H, W XXXXXXXX	IOWR2 [R/W] B, H, W XXXXXXXX	—	
00067C$_H$	—				
000680$_H$	CSER [R/W] B, H, W 00000001	—	—	TCR [W] B, H, W 0000XXXX	
000684$_H$ to 000AFC$_H$	—				Reserved
000B00$_H$	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXX	—	DSU (Evaluation chip only)
000B04$_H$	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11	
000B08$_H$	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX	

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block diagram
000B0CH	EWPT [R] 00000000 00000000		—		DSU (Evaluation chip only)
000B10H	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX		
000B14H to 000B1CH	—				
000B20H	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24H	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28H	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2CH	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30H	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34H	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38H	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3CH	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40H	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44H	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48H	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4CH	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50H	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5CH	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
000B64H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU (Evaluation chip only)
000B68H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6CH	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B70H to 000BFCH	—				Reserved
000C00H	Register access disallowed				Interrupt Control unit
000C04H to 000C14H	Register access disallowed				R-bus test
000C18H to 000FFCH	—				Reserved
001000H	DMASA0 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				DMAC
001004H	DMADA0 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001008H	DMASA1 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00100CH	DMADA1 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001010H	DMASA2 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001014H	DMADA2 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001018H	DMASA3 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00101CH	DMADA3 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001020H	DMASA4 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001024H	DMADA4 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001028H to 001FFCH	—				Reserved

(Continued)

(Continued)

Address	Register				Block diagram
	+ 0	+ 1	+ 2	+ 3	
007000H	FLCR [R/W] 0110X000	—	—	—	Flash memory
007004H	FLWC [R/W] 00010011	—	—	—	
007008H	—	—	—	—	
00700CH	—	—	—	—	
007010H	—	—	—	—	
007014H to 0070FFH	—				Reserved

*1 : Test register access barred

*2 : The lower 16-bit (DTC(15: 0)) of DMACA0 to DMACA4 cannot be accessed in byte.

*3 : The available area of internal RAM is restricted by the function described in 6-209 immediately after a reset is canceled. When the setting of the available area is updated, the instruction must be followed by at least 1 NOP instruction.

■ VECTOR TABLE

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	RN
	10	16				
Reset	0	00	—	3FC$_H$	000FFFFC$_H$	—
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$	—
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$	—
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$	—
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$	—
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$	—
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$	—
Instruction break exception	10	0A	—	3D4$_H$	000FFFD4$_H$	—
Operand break trap	11	0B	—	3D0$_H$	000FFFD0$_H$	—
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$	—
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	15 (F$_H$) fixed15	3C0$_H$	000FFFC0$_H$	—
External interrupt 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$	6
External interrupt 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$	7
External interrupt 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$	11
External interrupt 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$	—
External interrupt 4	20	14	ICR04	3AC$_H$	000FFFAC$_H$	—
External interrupt 5	21	15	ICR05	3A8$_H$	000FFFA8$_H$	—
External interrupt 6	22	16	ICR06	3A4$_H$	000FFFA4$_H$	—
External interrupt 7	23	17	ICR07	3A0$_H$	000FFFA0$_H$	—
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$	8
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$	9
Reload timer 2	26	1A	ICR10	394$_H$	000FFF94$_H$	10
UART(Reception completed)	27	1B	ICR11	390$_H$	000FFF90$_H$	0
UART(Reception completed)	28	1C	ICR12	38C$_H$	000FFF8C$_H$	1
UART(Reception completed)	29	1D	ICR13	388$_H$	000FFF88$_H$	2
UART0 (RX completed)	30	1E	ICR14	384$_H$	000FFF84$_H$	3
UART1 (RX completed)	31	1F	ICR15	380$_H$	000FFF80$_H$	4
UART2 (RX completed)	32	20	ICR16	37C$_H$	000FFF7C$_H$	5

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	RN
	10	16				
DMAC0 (end, error)	33	21	ICR17	378H	000FFF78H	—
DMAC1 (end, error)	34	22	ICR18	374H	000FFF74H	—
DMAC2 (end, error)	35	23	ICR19	370H	000FFF70H	—
DMAC3 (end, error)	36	24	ICR20	36CH	000FFF6CH	—
DMAC4 (end, error)	37	25	ICR21	368H	000FFF68H	—
A/D	38	26	ICR22	364H	000FFF64H	15
I^2C	39	27	ICR23	360H	000FFF60H	—
UART4 (Reception completed)	40	28	ICR24	35CH	000FFF5CH	—
SIO 5	41	29	ICR25	358H	000FFF58H	12
SIO 6	42	2A	ICR26	354H	000FFF54H	13
SIO 7	43	2B	ICR27	350H	000FFF50H	14
UART3 (Reception completed)	44	2C	ICR28	34CH	000FFF4CH	—
UART3 (RX completed)	45	2D	ICR29	348H	000FFF48H	—
Reload timer 3/main oscillation stabilization wait timer	46	2E	ICR30	344H	000FFF44H	—
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H	—
External interrupt: FPINT(8-15)	48	30	ICR32	33CH	000FFF3CH	—
Clock counter	49	31	ICR33	338H	000FFF38H	—
U/D Counter0	50	32	ICR34	334H	000FFF34H	—
U/D Counter1	51	33	ICR35	330H	000FFF30H	—
PPG 0/1	52	34	ICR36	32CH	000FFF2CH	—
PPG 2/3	53	35	ICR37	328H	000FFF28H	—
PPG 4/5	54	36	ICR38	324H	000FFF24H	—
16-bit free-run timer	55	37	ICR39	320H	000FFF20H	—
ICU2/3 (capture)	56	38	ICR40	31CH	000FFF1CH	—
ICU1 (capture)/UART4 (transmission complete)	57	39	ICR41	318H	000FFF18H	—
ICU0 (capture)	58	3A	ICR42	314H	000FFF14H	—
OCU0/1 (match)	59	3B	ICR43	310H	000FFF10H	—
OCU2/3 (match)	60	3C	ICR44	30CH	000FFF0CH	—
OCU4/5 (match)	61	3D	ICR45	308H	000FFF08H	—
OCU6/7 (match)	62	3E	ICR46	304H	000FFF04H	—
Interrupt delay source bit	63	3F	ICR47	300H	000FFF00H	—
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH	—
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	RN
	10	16				
System reserved	66	42	—	$2F4_H$	$000FFEF4_H$	—
System reserved	67	43	—	$2F0_H$	$000FFEF0_H$	—
System reserved	68	44	—	$2EC_H$	$000FFEEC_H$	—
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$	—
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$	—
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$	—
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$	—
System reserved	73	49	—	$2D8_H$	$000FFED8_H$	—
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$	—
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$	—
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$	—
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$	—
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$	—
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$	—
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$	—

■ PERIPHERAL RESOURCES

1. Interrupt controller

(1)Description

The interrupt controller manages interrupt reception and arbitration.

• Hardware configuration

This module consists of the following components:
- ICR register
- Interrupt priority determination circuit
- Interrupt level and interrupt number (vector) generator
- HOLD request cancellation request generator

• Main function

This module has the following major functions:
- Detect NMI and interrupt requests
- Prioritize interrupts (according to level and number)
- Notify interrupt level of selected interrupt request (to CPU)
- Notify interrupt number of selected interrupt request (to CPU)
- Request (to the CPU) to return from stop mode in response to an NMI or interrupt request with interrupt level other than “11111”
- Hold request cancellation request issued to the bus master

(2)Register list

ICR register

	7	6	5	4	3	2	1	0
ICR00	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR01	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR02	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR03	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR04	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR05	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR06	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR07	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR08	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR09	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR10	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR11	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR12	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR13	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR14	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR15	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0

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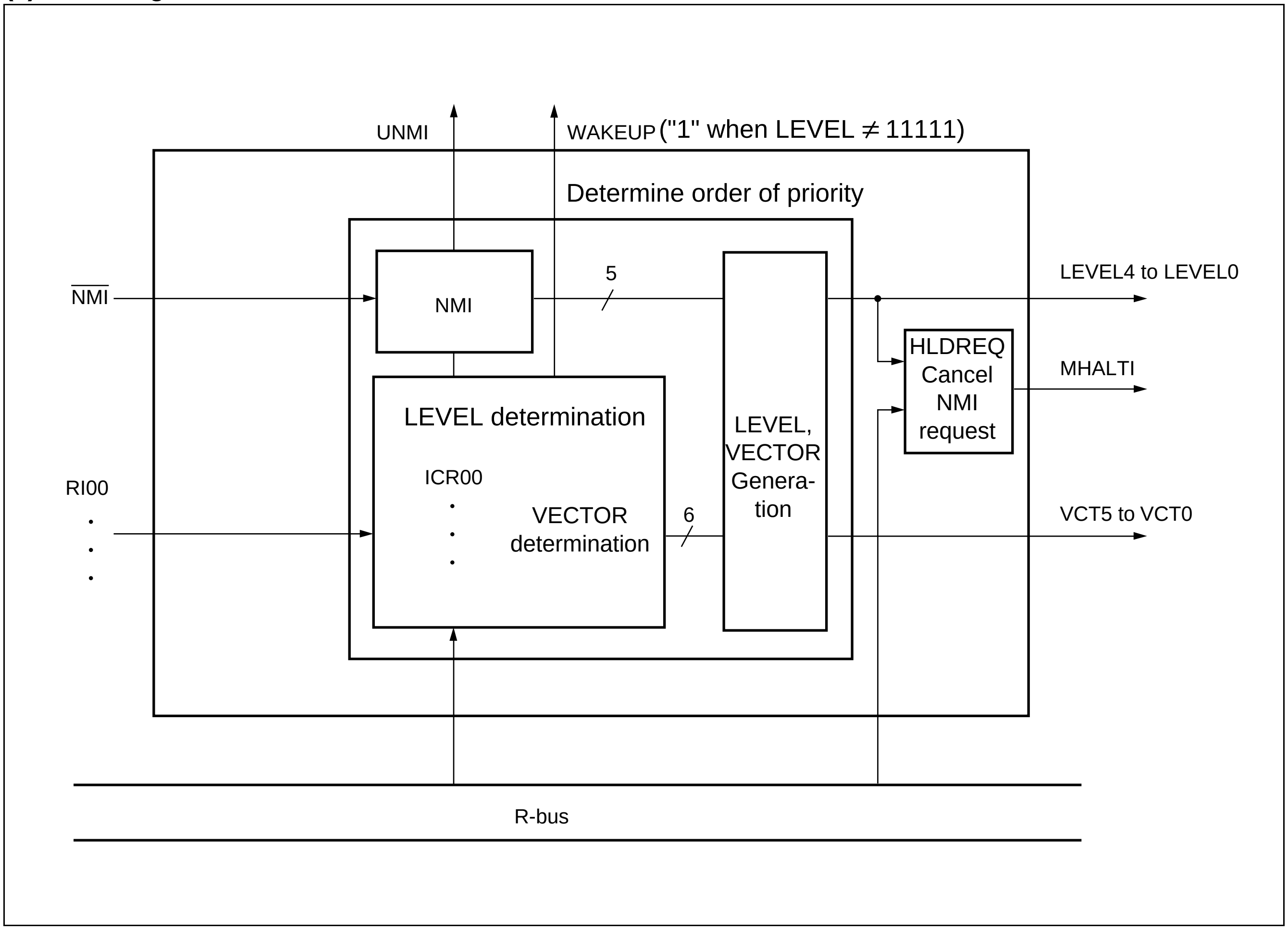
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	7	6	5	4	3	2	1	0
ICR16	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR17	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR18	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR19	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR20	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR21	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR22	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR23	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR24	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR25	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR26	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR27	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR28	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR29	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR30	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR31	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR32	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR33	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR34	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR35	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR36	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR37	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR38	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR39	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR40	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR41	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR42	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR43	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR44	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR45	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR46	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR47	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0

Hold request cancel request resister (HRCL)

	7	6	5	4	3	2	1	0
HRCL	MHALT1	—	—	LVL4	LVL3	LVL2	LVL1	LVL0

(3)Block diagram



2. External interrupt/NMI control

(1)Description

The external interrupt control unit is the block that controls external interrupt requests input to $\overline{\text{NMI}}$ and INT0 to INT15.

The level can be selected from “H”, “L”, rising edge, or falling edge (except for NMI).

(2)Register list

External interrupt enable register (ENIR)

7	6	5	4	3	2	1	0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

External interrupt request register (EIRR)

15	14	13	12	11	10	9	8
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

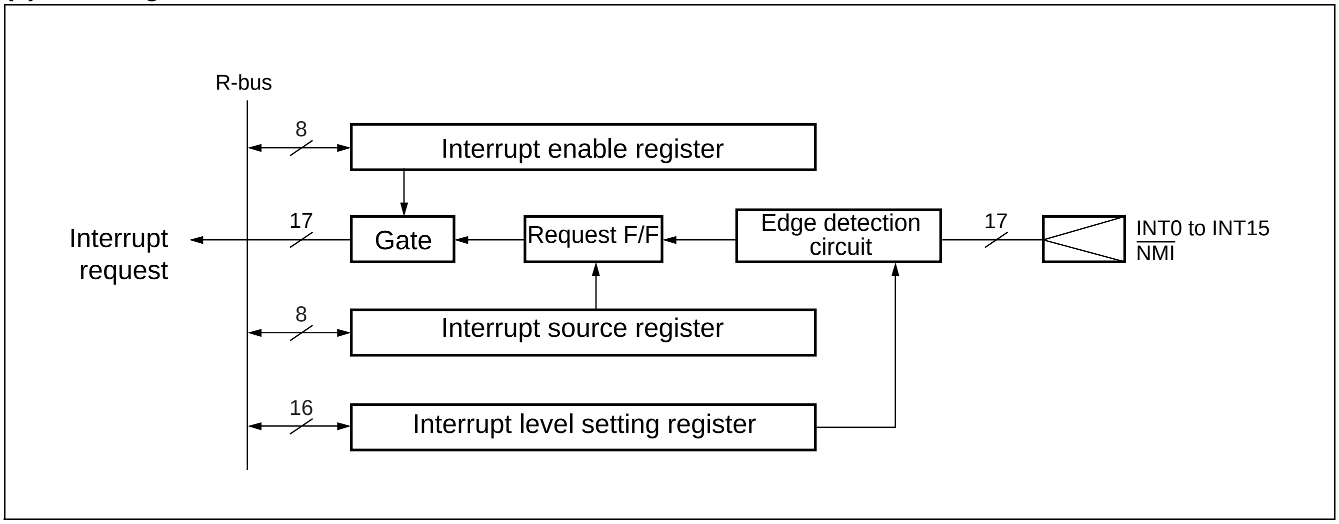
Request level setting register (ELVR)

15	14	13	12	11	10	9	8
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

7	6	5	4	3	2	1	0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

The above registers (for 8 channels) are available in two sets; there are a total of 16 channels.

(3)blockdiagram



3. REALOS-related Hardware

REALOS-related hardware is used by the real-time OS. Therefore, REALOS-related hardware cannot be used by user programs when REALOS is used.

• Delay interrupt module

(1)Description

The delayed interrupt module generates a task switching interrupt.

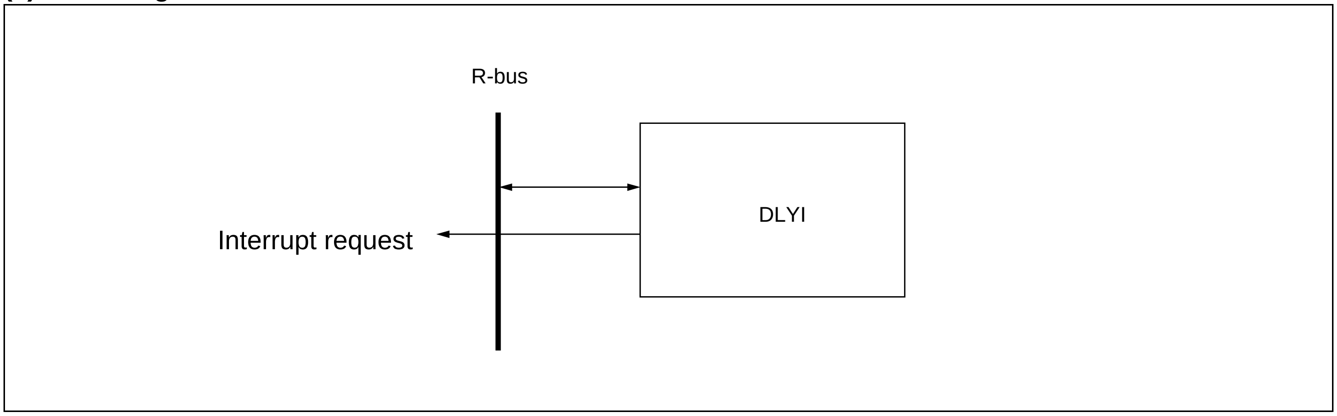
This module enables software to issue or cancel an interrupt request to the CPU.

(2)Register list

Delayed Interrupt Control Register (DICR)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	DLY1

(3)Block diagram



• **Bit Search Module**

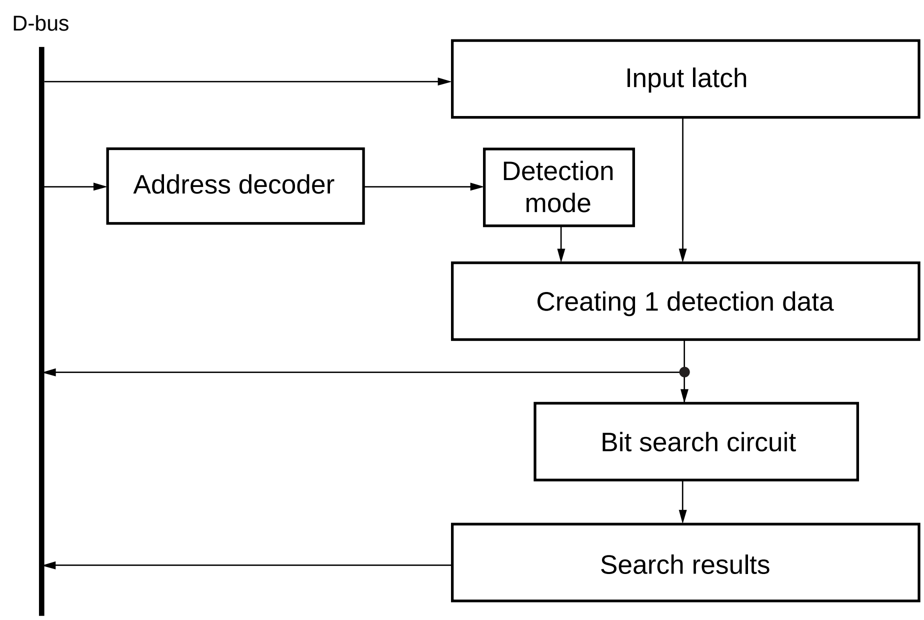
(1)Description

The bit search module searches data written to an input register for “0”, “1”, or a change point and returns the detected bit position.

(2)Register list

	31 0
0 detection data register (BSD0)	
1 detection data register (BSD1)	
Data register for transition detection (BSDC)	
Detection result register (BSRR)	

(3)Block diagram



4. 8/16-bit up/down counter

(1)Description

This block is the up/down counter consisting of 6 event input pins, an 8/16-bit up/down counter, an 8-bit reload/compare register, and their control circuit.

The MB91F355A/MB91F356B/MB91355A/MB91354A/MB91V350A contain 2 channels of 8/16-bit up/down counter in this block.

This module has the following features.

- 8-bit count register enabling counting from (0)d to (255)d (enabling counting from (0)d to (65535)d in "16-bit x 1 operation mode").
- Four different count modes available with selectable count clocks

  Count mode
  - Timer mode
  - Up/down counter mode
  - Phase difference count mode (2 multiplication)
  - Phase difference count mode (4 multiplication)

- Capable of selecting a count clock signal in timer mode, from among the inputs from two internal clocks and an internal circuit

  Count clock (When operating at 25 MHz)
  - 80 ns (12.5 MHz : 2-frequency division)
  - 320 ns (3.125 Hz : 8-frequency division)

- Capable of selecting the detection edge of the external pin input signal in up/down counter mode

  Detection edge
  - Falling Edge detection
  - Rising Edge detection
  - Detection at rising edge, falling edge, or both edges
  - Edge detection disabled

- Phase difference count mode suitable for counting for an encoder such as a motor, capable of easily counting the rotation angle and the number of revolutions at high precision by inputting the phase-A, phase-B, and phase-Z outputs of the encoder
- ZIN pin available for two functions selectable (valid in all modes)

  ZIN Pin
  - Counter clear function
  - Gate function

- Compare and reload functions available not only separately but also in combination for up/down counting at an arbitrary width

  Compare/reload function
  - Compare function (comparison interrupt request output)
  - Compare function (comparison interrupt request output and counter clear)
  - Reload function (underflow interrupt request output and reload)
  - Compare/reload function(Comparison interrupt request output and counter clear; underflow interrupt request output and reload)
  - Compare/reload disabled

- Count direction flag used to identify the preceding count direction
- Capable of controlling the independent generations of interrupts at a compare match, reload (underflow), overflow, or at a count direction change

(2)Register list

• Up/down count resister (UDCR)

Up/down count resister ch0 (UDCR0)

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00

Up/down count resister ch1 (UDCR1)

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D09	D08

• Reload compare resister (RCR)

Reload compare resister ch0 (RCR0)

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00

Reload compare resister ch1 (RCR1)

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D09	D08

• Counter status register (CSR)

Counter status register ch(0, 1) (CSR0, 1)

7	6	5	4	3	2	1	0
CST	CIT	UDI	CM	OVF	UD	UD	UD

• Counter control resister (CCRL)

Counter control resister ch(0, 1) (CCRL0, 1)

7	6	5	4	3	2	1	0
Reserved	CTU	UC	RLD	UD	CGS	CGE	CGE

• Counter control resister (CCRH)

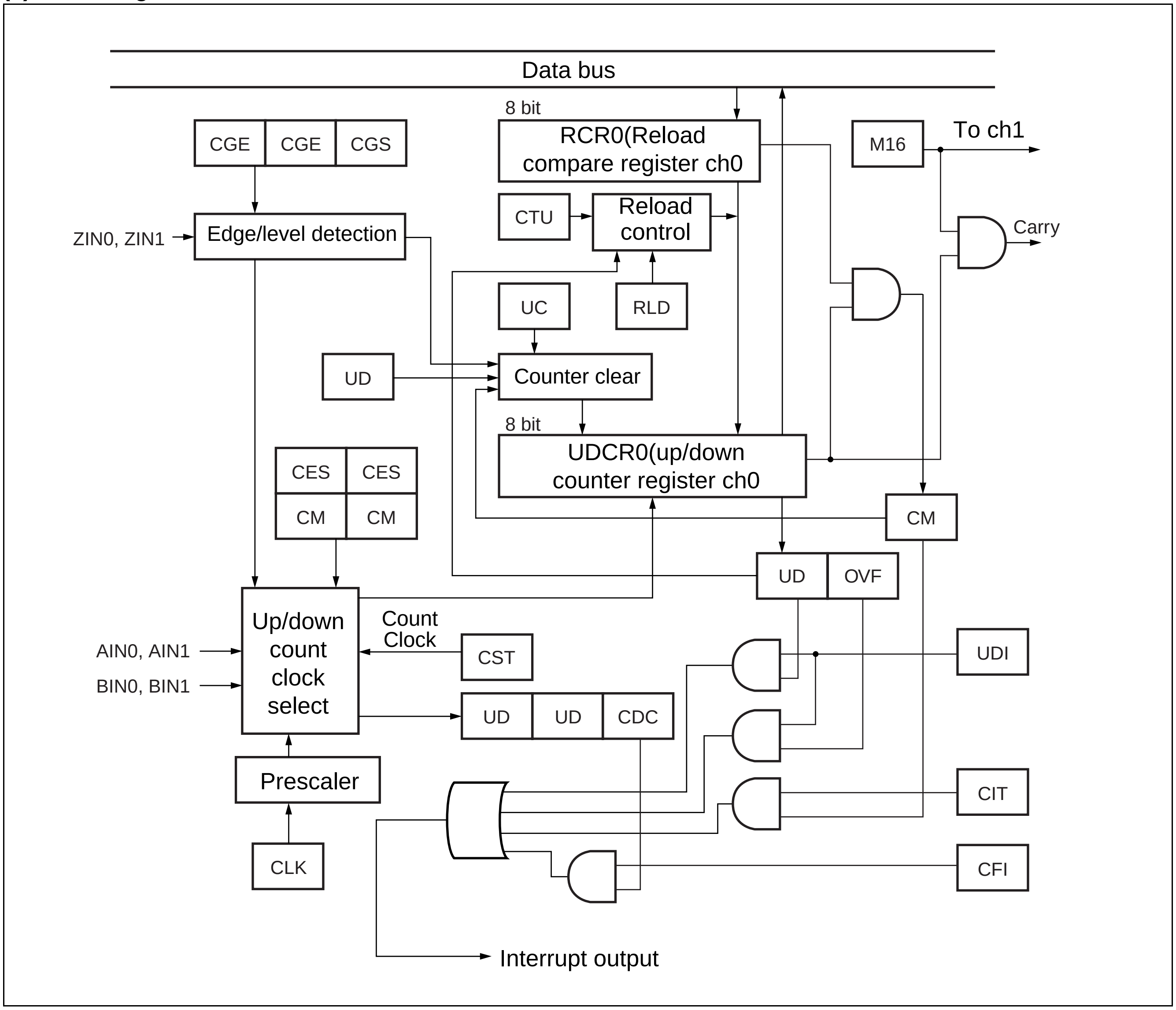
Counter control resister ch0 (CCRH0)

15	14	13	12	11	10	9	8
M16	CDC	CFI	CLK	CM	CM	CES	CES

• Counter control resister ch1 (CCRH1)

15	14	13	12	11	10	9	8
Reserved	CDC	CFI	CLK	CM	CM	CES	CES

(3)Block diagram



5. 16-bit Reload Timer

(1)Description

The 16-bit timer consists of a 16-bit down counter, 16-bit reload register, internal clock, clock generation prescaler, and control register.

The clock source can be selected from among three internal clocks (prepared by frequency dividing the machine clock by 2/8/32, and also by 64/128 only for ch3) and an external event.

The interrupt can be used to initiate DMA transfer.

The MB91F355A/MB91F356B/MB91355A/MB91354A/MB91V350A contain 4 channels of this timer.

(2)Register list

Control status register (TMCSR)

15	14	13	12	11	10	9	8
—	—	Reserved	CSL2	CSL1	CSL0	Reserved	Reserved

(ch3 only)

7	6	5	4	3	2	1	0
Reserved	—	OUTL	RELD	INTE	UF	CNTE	TRG

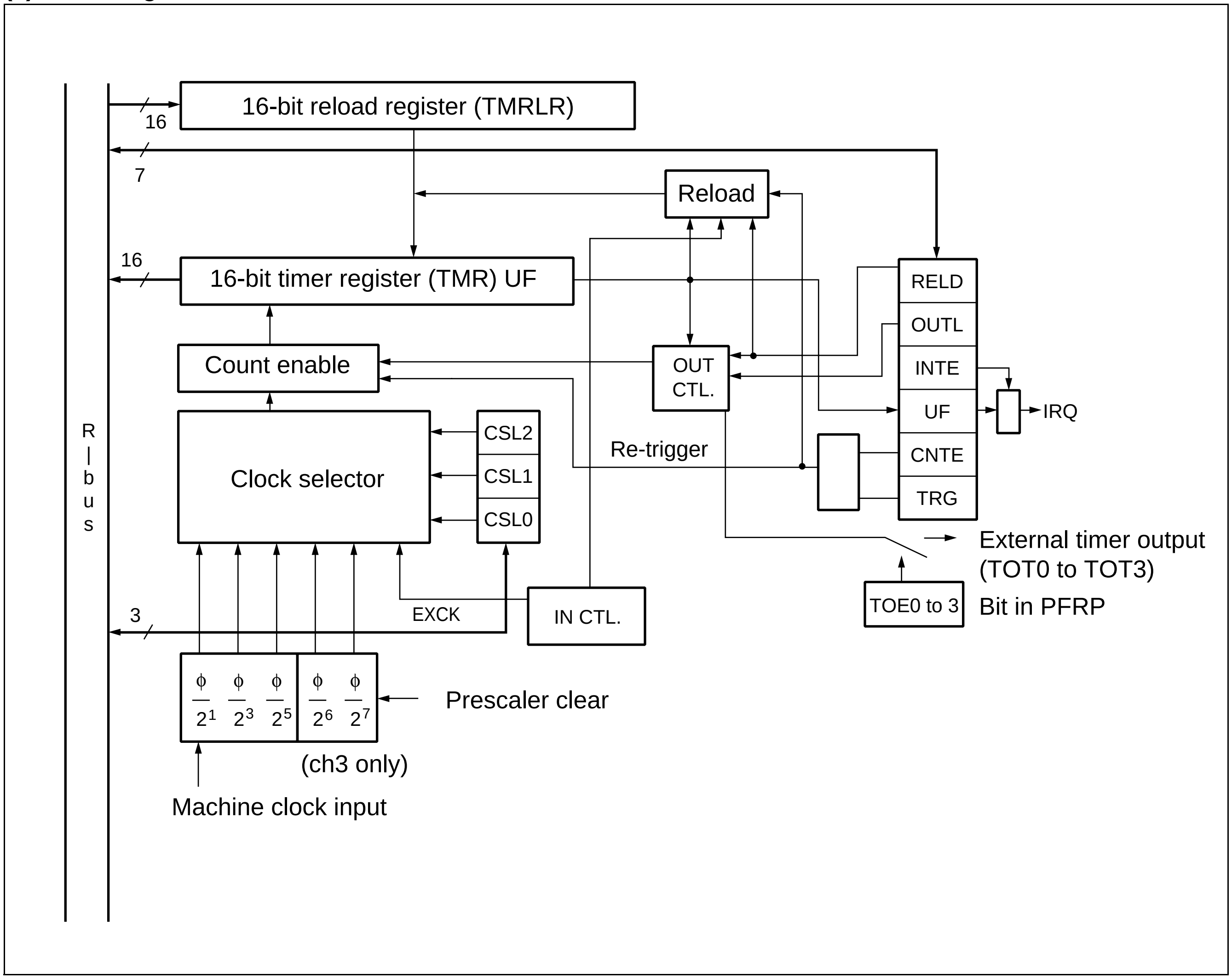
16-bit timer register(TMR)

15 … 0

16-bit reload register(TMRLR)

15 … 0

(3)Block diagram



6. PPG (Programable Pulse Generator)

The PPG can efficiently output highly precise PWM waveforms.
The MB91F355A/MB91F356B/MB91355A/MB91354A/MB91V350A contain 6 channels of PPG timer.

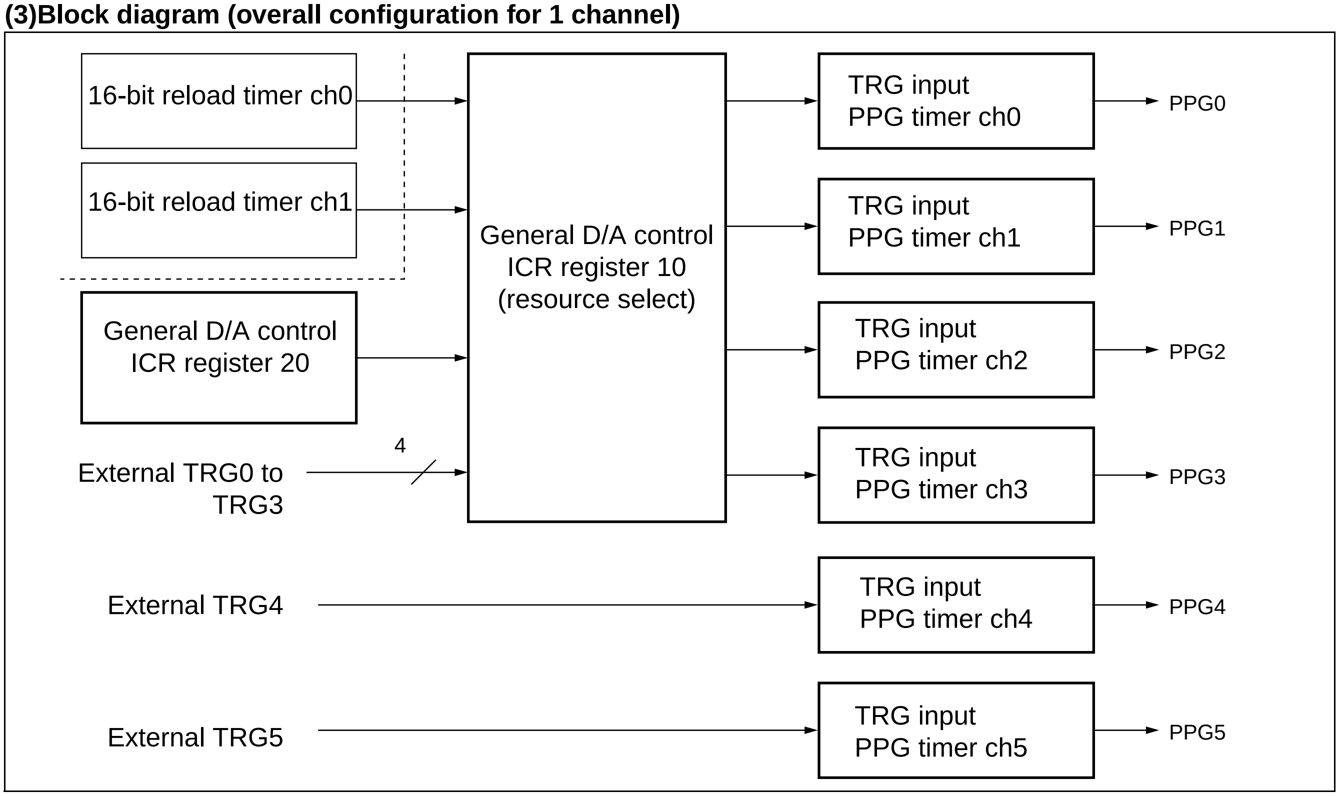
(1)Description

Each channel consists of a 16-bit down counter, 16-bit data register with cycle setting buffer, 16-bit compare register with duty ratio setting buffer, and pin control unit.
The count clocks for the 16-bit down counter can be selected from the following 4 types :(peripheral clock ϕ, ϕ/4, ϕ/16, ϕ/64)
The counter is initialized to "FFFF$_H$" at a reset or counter borrow.
PPG outputs (PPG0 to PPG5) are provided for each channel.

(2)Register list

Register	15 … 0
General control register 10 (GCN10)	
General control register 20 (GCN20)	
Timer register (PTMR0 to 5)	
Cycle setting register (PCSR0 to 5)	
Duty setting register (PDUT0)	

(3)Block diagram (overall configuration for 1 channel)

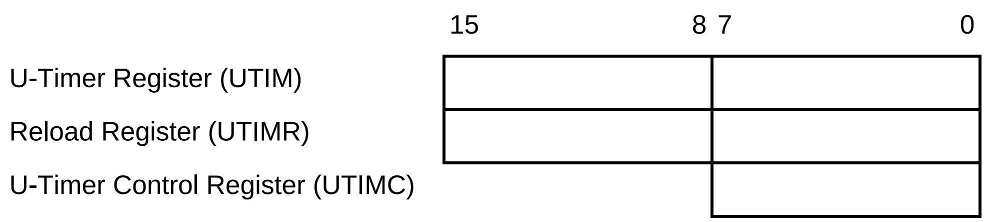


7. U-Timer (16-bit timer for UART baud rate generation)

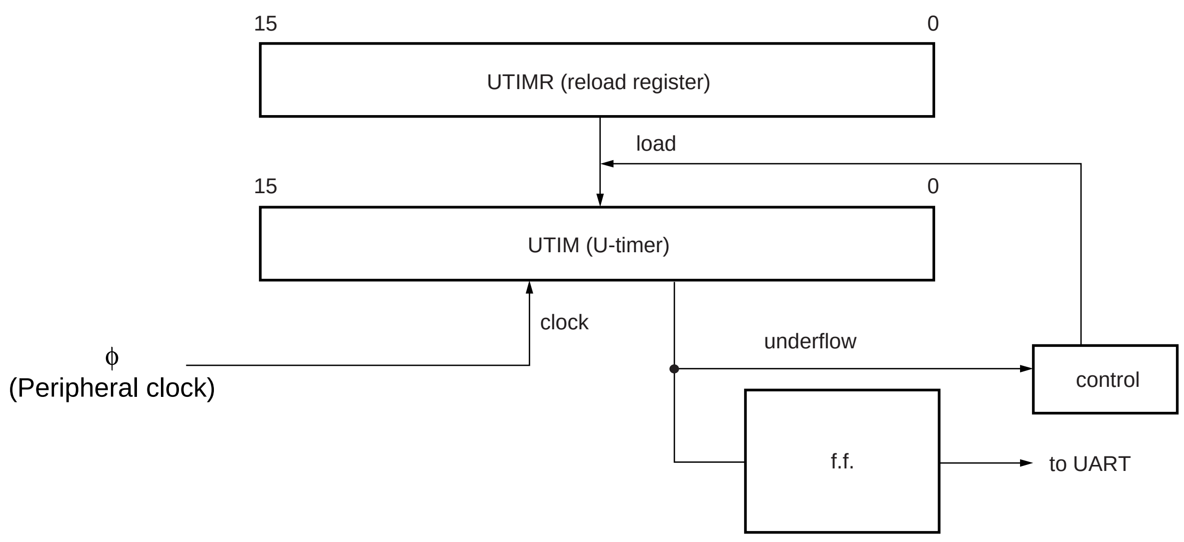
(1) Description

The U-Timer is a 16-bit timer for generating the baud rate for the UART. An arbitrary baud rate can be set depending on the combination of the chip operating frequency and U-Timer reload value.
The MB91F355A/MB91F356B/MB91355A/MB91354A/MB91V350A contain 5 channels of this timer.

(2) Register list



(3) Block diagram



8. UART

(1) Description

The UART is a serial I/O port for asynchronous (start-stop) or CLK synchronous communication. This module has the features listed below. The MB91F355A/MB91F356B/MB91355A/MB91354A/MB91V350A contain 5 channels of UART.

- Full duplex double buffer
- Asynchronous (start-stop synchronized) or CLK synchronized transmission
- Supports multi-processor mode
- Completely programmable baud rate.
  Arbitrary baud rate set by built-in timer (See the section for "U-Timer".)
- Variable baud rate can be input from an external clock.
- Error detection functions(parity, framing, overrun)
- Transmission signal format is NRZ
- UART Ch0 to Ch2 can start DMA transfer using interrupts (Ch3 and Ch4 cannot start DMA transfer).
- Capable of clearing DMAC interrupt source by writing to DRCL register

(2)Register list

Serial input register/serial output register (SIDR/SODR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Serial status register(SSR)

7	6	5	4	3	2	1	0
PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE

Serial mode register

7	6	5	4	3	2	1	0
MD1	MD0	—	—	CS0	—	—	—

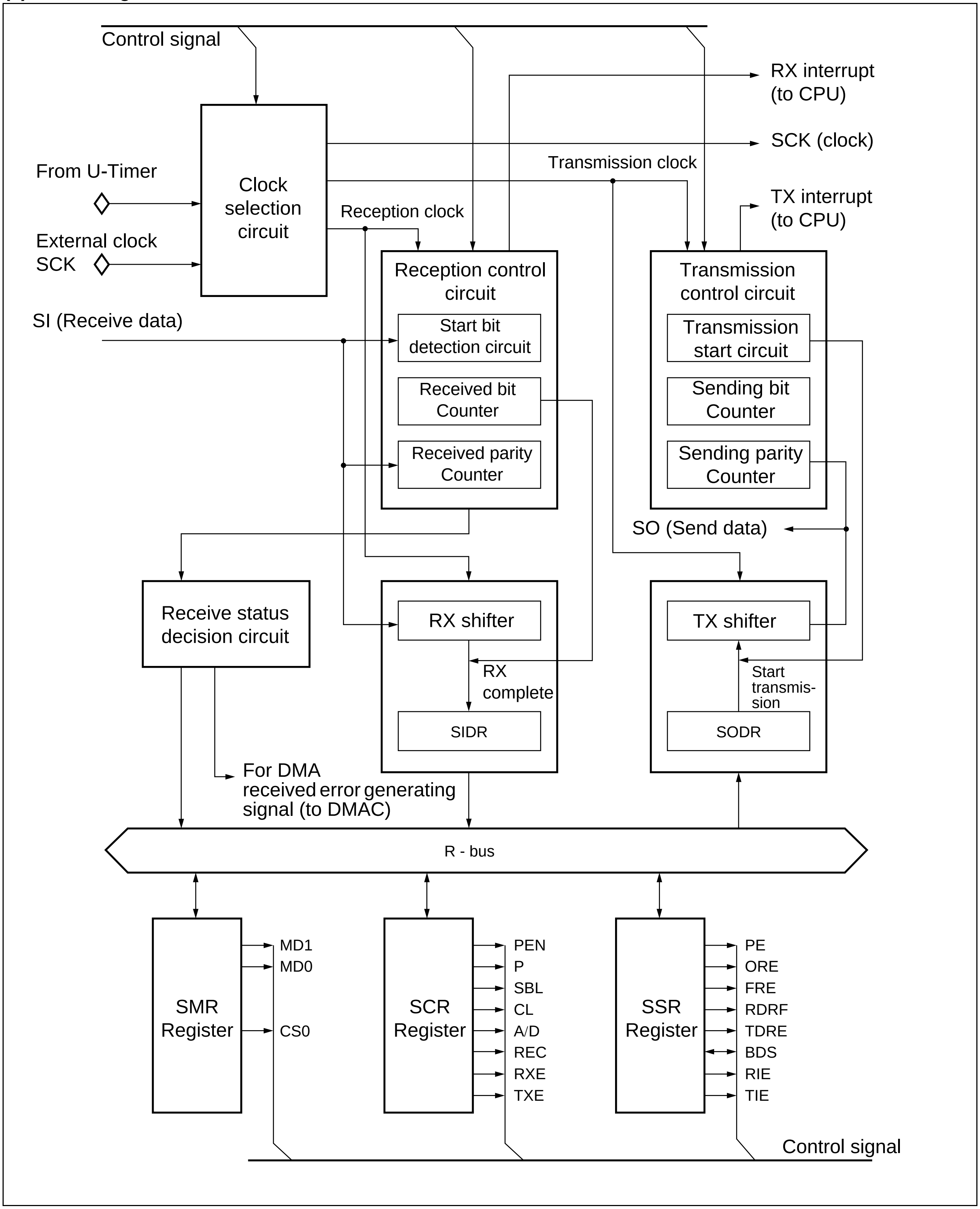
Serial control register(SCR)

7	6	5	4	3	2	1	0
PEN	P	SBL	CL	A/D	REC	RXE	TXE

DECL register (DRCL)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

(3) Block diagram



9. Extended I/O Serial Interface (SIO)

(1) Description

This block is a serial I/O interface that allows data transfer using clock synchronization. It is composition of a single 8-bit × 1 channel.
LSB-first or MSB-first transfer mode can be selected for data transfer.
The MB91F355A/MB91F356B/MB91355A/MB91354A/MB91V350A contain 3 channels of this SIO.

The serial I/O interface operates in 2 modes:

- Internal shift clock mode: Transfer data in synchronization with the internal clock.
- External shift clock mode: Transfer data in synchronization with the clock supplied via the external pin (SCK). By manipulating the general-purpose port sharing the external pin (SCK) in this mode, data can also be transferred by a CPU instruction.

(2) Register list

Serial mode control status register (SMCS)

15	14	13	12	11	10	9	8
SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT

7	6	5	4	3	2	1	0
—	—	—	—	MODE	BDS	—	—

SIO test resister(SES)

15	14	13	12	11	10	9	8
—	—	—	—	—	—	TST1	TST0

SDR (Serial Data Register)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

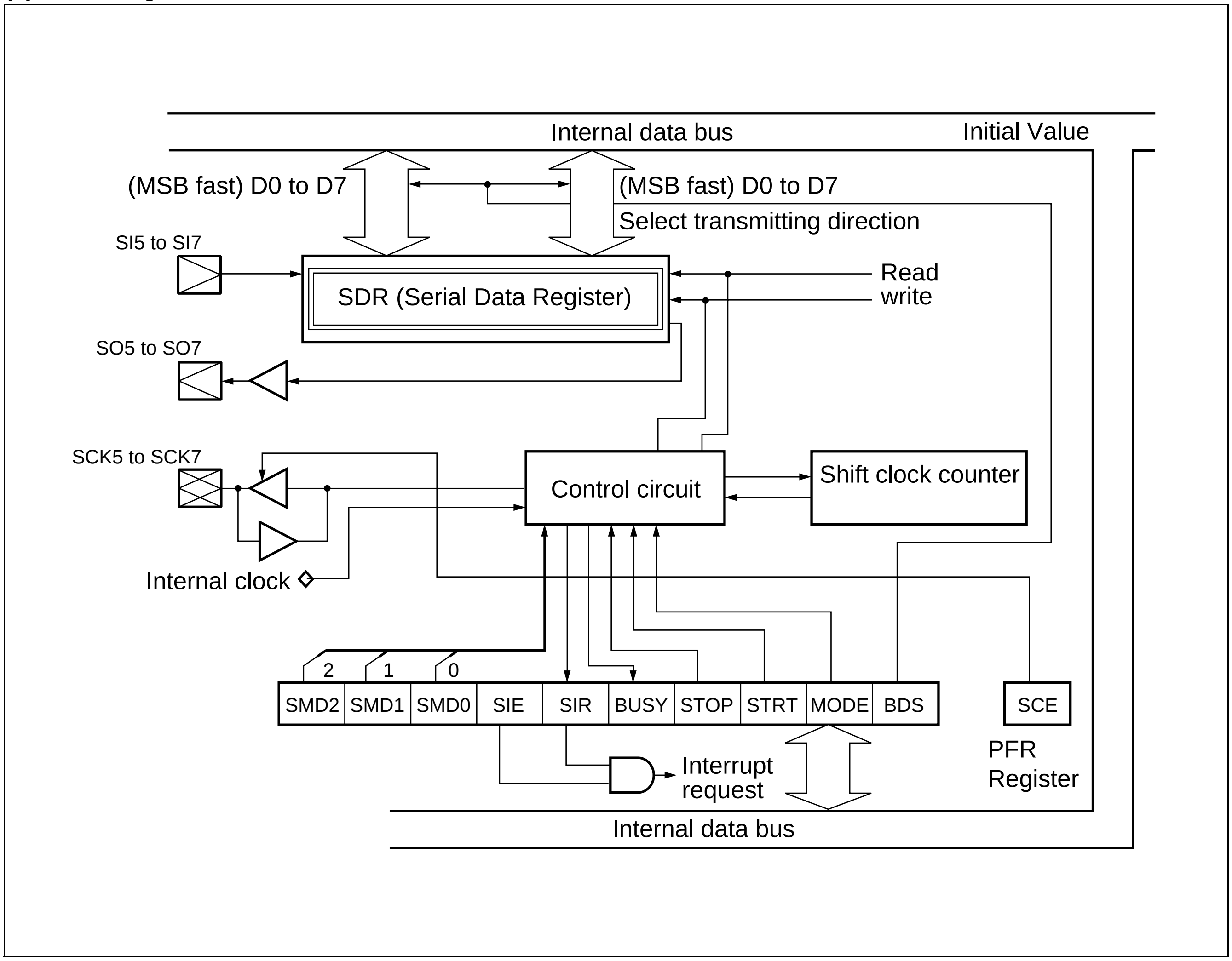
SIO prescaler control register (CDCR)

15	14	13	12	11	10	9	8
MD	—	—	—	DIV3	DIV2	DIV1	DIV0

DMAC interrupt source clear register (SRCL)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

(3)Block diagram



10. 16-bit free-run timer

(1)Description

The 16-bit free-running timer consists of a 16-bit up counter, control register, and status register. The count values of this timer are used as the base timer for the output compares and input capture modules.

- Four count clock frequencies are available.
- An interrupt can be generated at a counter overflow.
- The counter can be initialized upon a match with compare register 0 of the output compare unit, depending on the mode.

(2)Register list

Timer data register (upper) (TCDT)

15	14	13	12	11	10	9	8
T15	T14	T13	T12	T11	T10	T9	T8

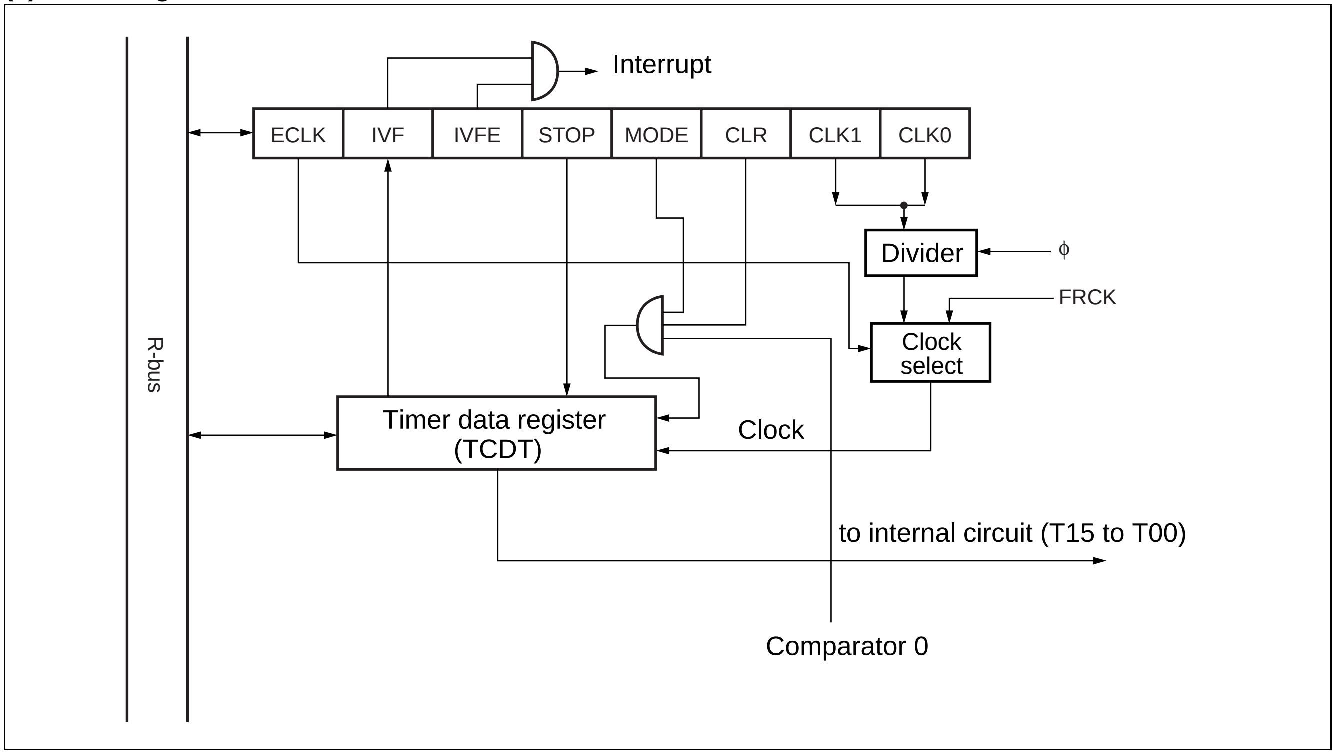
Timer data register (lower) (TCDT)

7	6	5	4	3	2	1	0
T07	T06	T05	T04	T03	T02	T01	T00

Timer control status register (lower) (TCCS)

7	6	5	4	3	2	1	0
ECLK	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0

(3)Block diagram



11. Input Capture

(1) Description

This module detects a rising or falling edge or both edges of an external input signal and stores the 16-bit free-running timer value in a register.

This module stores the 16-bit free-running timer value in a register. In addition, the module can generate an interrupt upon detection of an edge.

The input capture module consists of input capture data registers and a control register.

Each input capture unit has a corresponding external input pin.

- The detection edge of an external input can be selected from among 3 types.

  Rising edge

  Falling edge

  Both edges
- An interrupt can be generated upon detection of a valid edge of an external input.

(2) Register list

Input capture data register (upper) (IPCP)

15	14	13	12	11	10	9	8
CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08

Input capture data register (lower) (IPCP)

7	6	5	4	3	2	1	0
CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00

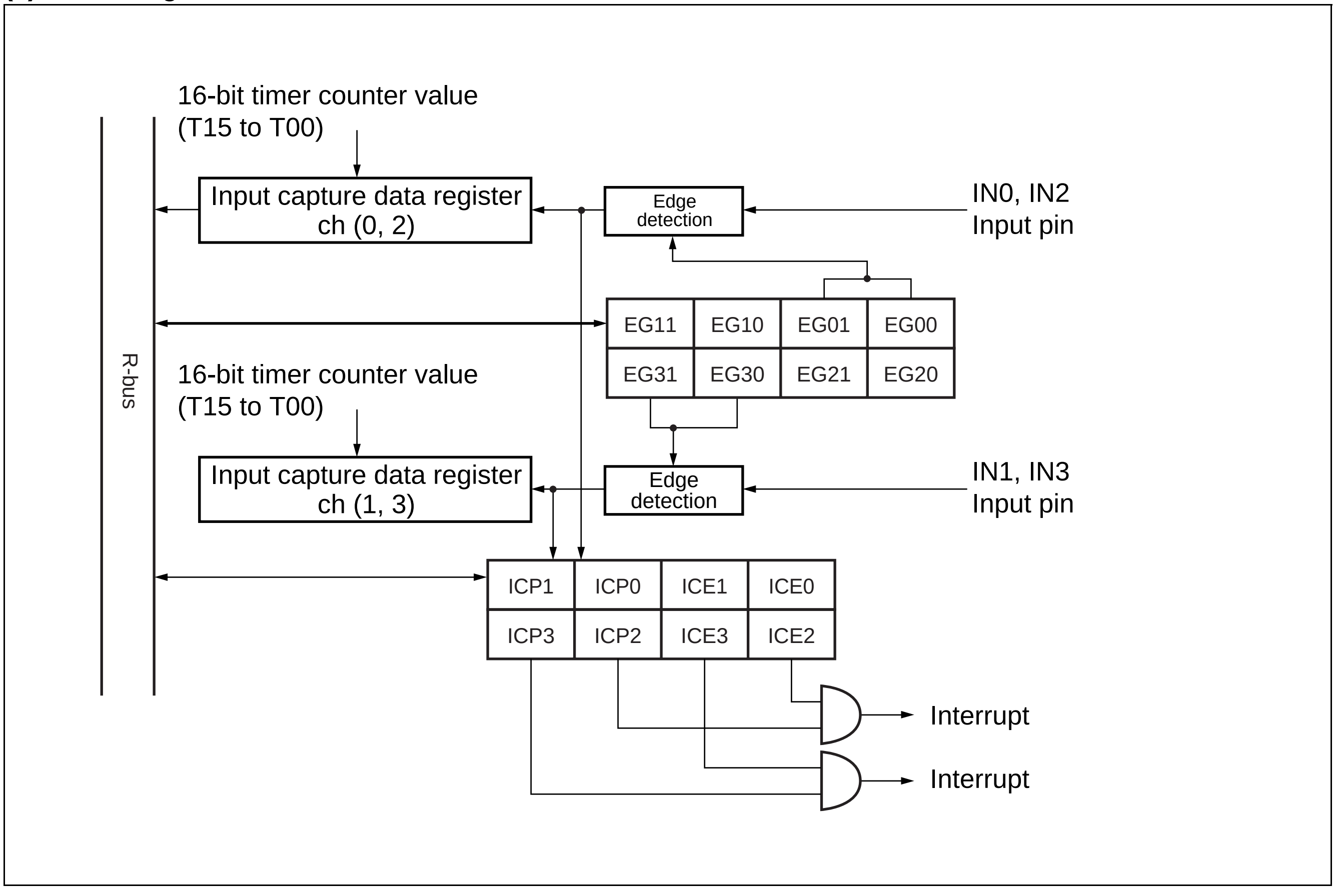
Capture control register (ICS23)

7	6	5	4	3	2	1	0
ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20

Capture control register (ICS01)

7	6	5	4	3	2	1	0
ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00

(3) Block diagram



12. Output Compare

(1) Description

The output compare module consists of 16-bit compare registers, compare output latch, and control register. When the 16-bit free-running timer value matches the compare register value, the output level is inverted and an interrupt is issued.
The MB91F355A/MB91F356B/MB91355A/MB91354A/MB91V350A contain 8 channels of this block.

This module has the features listed below.

- Capable of using the 8 compare registers independently. Output pins and interrupt flags corresponding to the compare registers
- A pair of compare registers can be used to control output pins. Using tow compare registers to invert output pins
- Capable of setting the initial value for each output pin.
- Interrupts can be generated upon a compare match.
- The ch0 compare register is used as the compare clear register for the 16-bit free-running timer.

(2)Register list

Output compare register(upper) (OCCP)

15	14	13	12	11	10	9	8
C15	C14	C13	C12	C11	C10	C09	C08

Output compare register(lower) (OCCP)

7	6	5	4	3	2	1	0
C07	C06	C05	C04	C03	C02	C01	C00

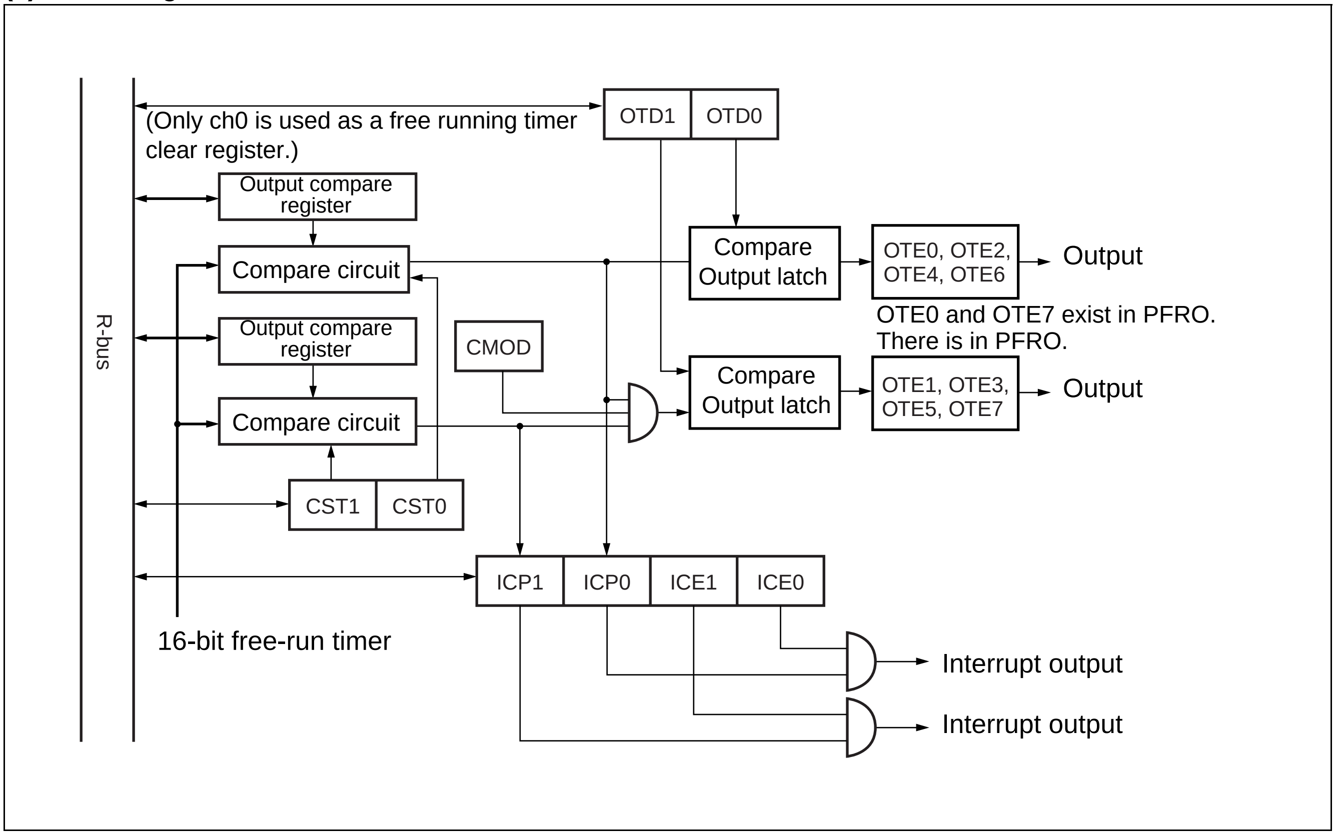
Output control register(upper) (OCS)

15	14	13	12	11	10	9	8
—	—	—	CMOD	—	—	OTD1	OTD0

Output control register(lower) (OCS)

7	6	5	4	3	2	1	0
ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0

(3) Block diagram



13. I²C Interface

(1) Description

The I²C interface is a serial I/O port supporting the Inter-IC bus, operating as a master/slave device on the I²C bus. It has the following features

- Master/slave sending and receiving
- Arbitration function
- Clock sync function
- Slave address and general call address detection function
- Ditecting function of transmitting direction
- Repeated start condition generation and detection function
- Bus error detection function
- 10-bit/7-bit slave address
- Slave address receive acknowledge control when in master mode
- Support for composite slave addresses
- Capable of interruption when a transmission or bus error occurs
- Standard mode (Max 100K bps)/High speed mode (Max 400K bps) supported

(2)Register list

Bus control register(IBCR)

15	14	13	12	11	10	9	8
BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT

Bus status register(IBSR)

7	6	5	4	3	2	1	0
BB	RSC	AL	LRB	TRX	AAS	GCA	ADT

10-bit slave address resister (ITBA)

15	14	13	12	11	10	9	8
—	—	—	—	—	—	TA9	TA8

7	6	5	4	3	2	1	0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

10-bit slave address mask resister(ITMK)

15	14	13	12	11	10	9	8
ENTB	RAL	—	—	—	—	TM9	TM8

7	6	5	4	3	2	1	0
TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

7-bit slave address resister (ISBA)

7	6	5	4	3	2	1	0
—	SA6	SA5	SA4	SA3	SA2	SA1	SA0

7-bit slave address mask resister (ISMK)

15	14	13	12	11	10	9	8
ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0

Data register (IDAR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

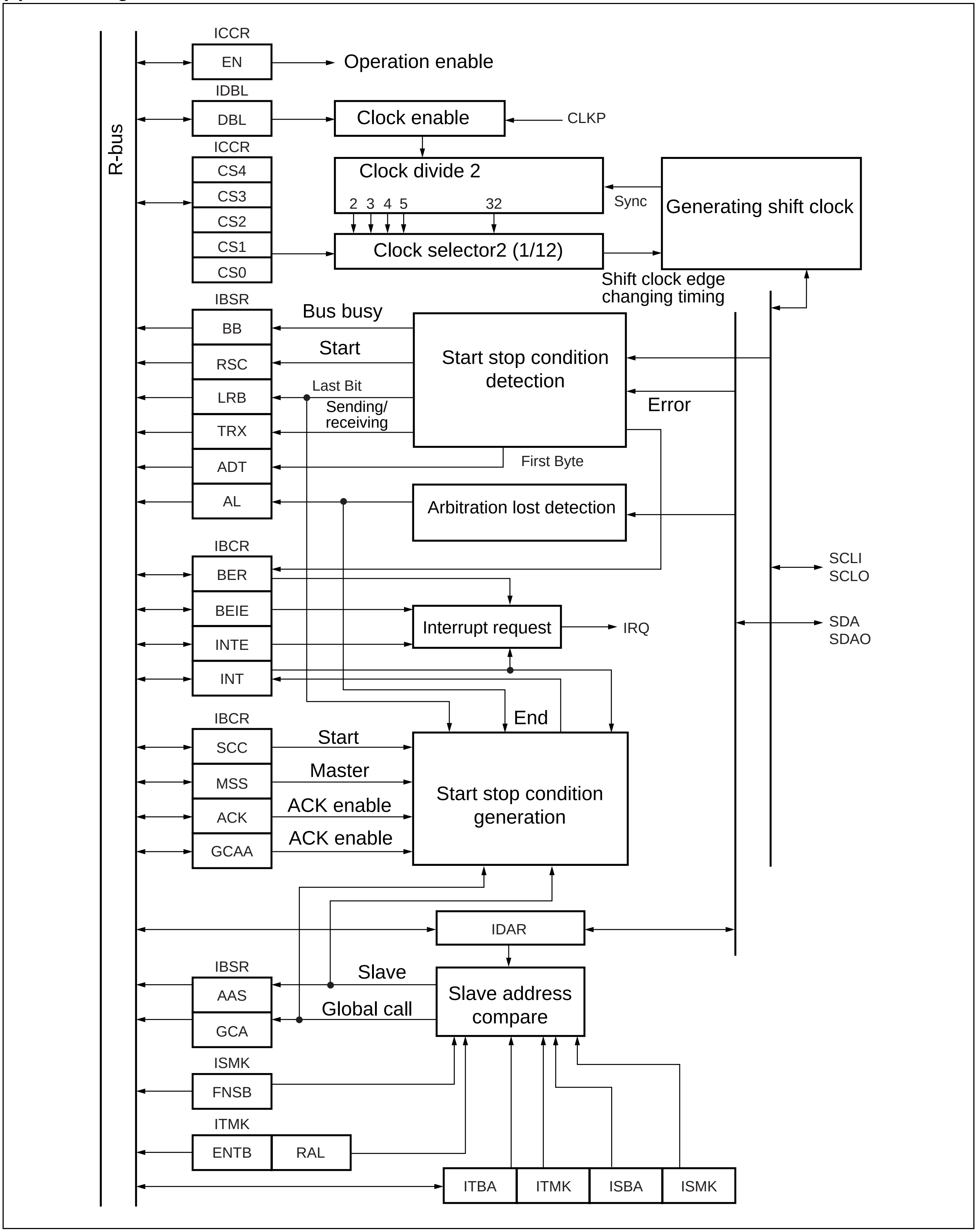
Clock control register (ICCR)

15	14	13	12	11	10	9	8
TEST	—	EN	CS4	CS3	CS2	CS1	CS0

Clock disable register (IDBL)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	DBL

(3) Block diagram



14. A/D Converter

(1) Description

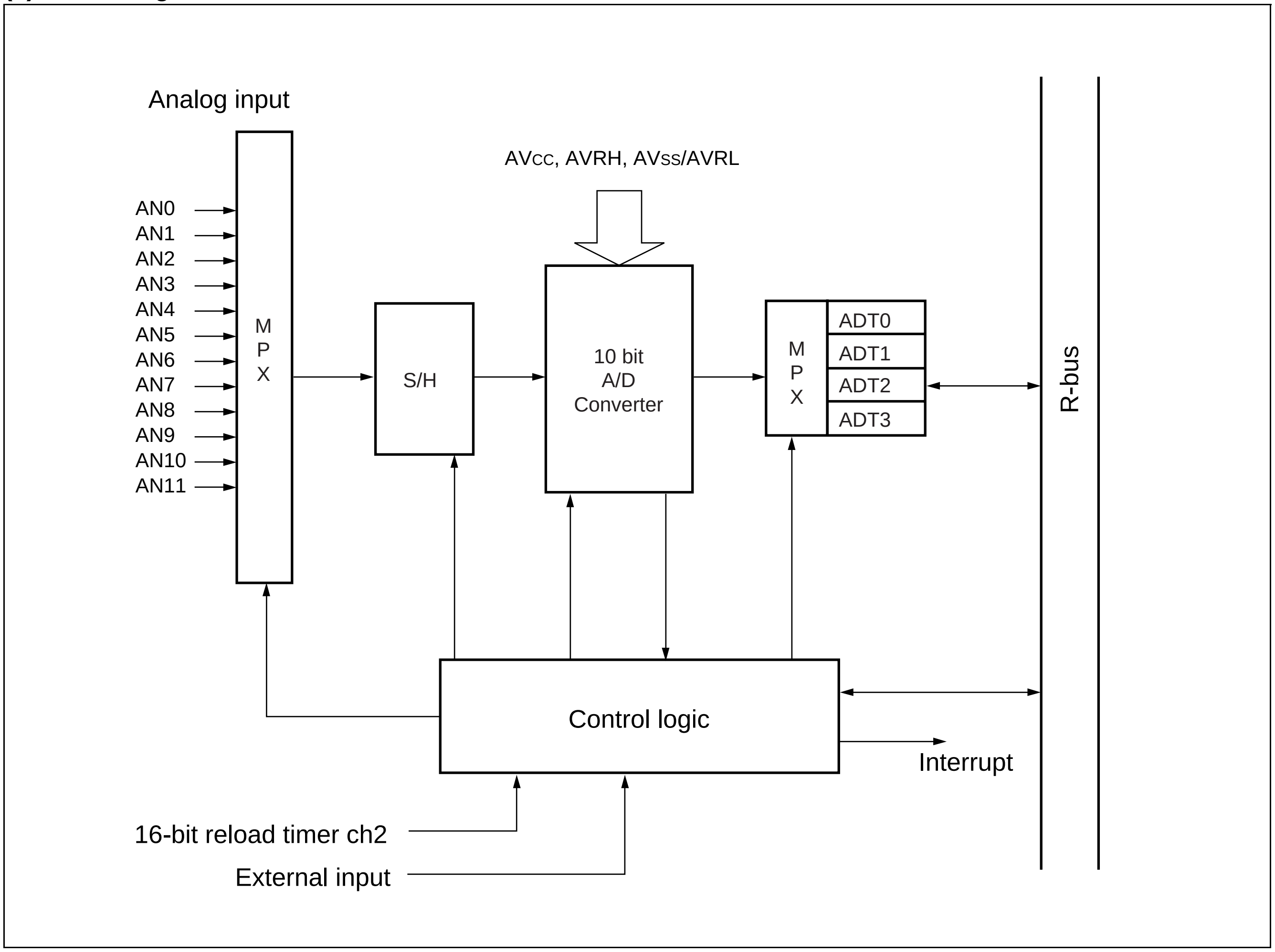
The A/D converter converts the analog input voltage into a digital value. It has the following features:

- Conversion time: 1.48 µs minimum per channel
- Employing serial/parallel conversion type for sample & hold circuit
- 10-bit resolution (switchable between 8 and 10 bits)
- Program selection of the analog input from among 12 channels
- Conversion mode
  Single conversion mode : Convert 1 selected channel
  Scan conversion mode : Scan up to 4 channels.
- Converted data is stored in the data buffer.
- An interrupt request to the CPU can be generated upon completion of A/D conversion. The interrupt can be used to start DMA transfer.
- The startup source can be selected from among software, external trigger (falling edge), and reload timer ch2 (rising edge).

(2) Register list

	15 — 8	7 — 0
Control status register (ADCS2/ADSC1)	ADCS2	ADCS1
Conversion time setting resister (ADCT)		
Converted data register 0 (ADTH0/ADTL0)	ADTH0	ADTL0
Converted data register 1 (ADTH1/ADTL1)	ADTH1	ADTL1
Converted data register 2 (ADTH2/ADTL2)	ADTH2	ADTL2
Converted data register 3 (ADTH3/ADTL3)	ADTH3	ADTL3

(3) Block diagram



15. 8-bit D/A Converter

(1) Description

This block contains 2 channels of 8-bit D/A converters. The D/A converter register can be used to control the independent output of each channel. The block has the following features.

- Power saving function
- 3.3 V Interface

(2) Register list

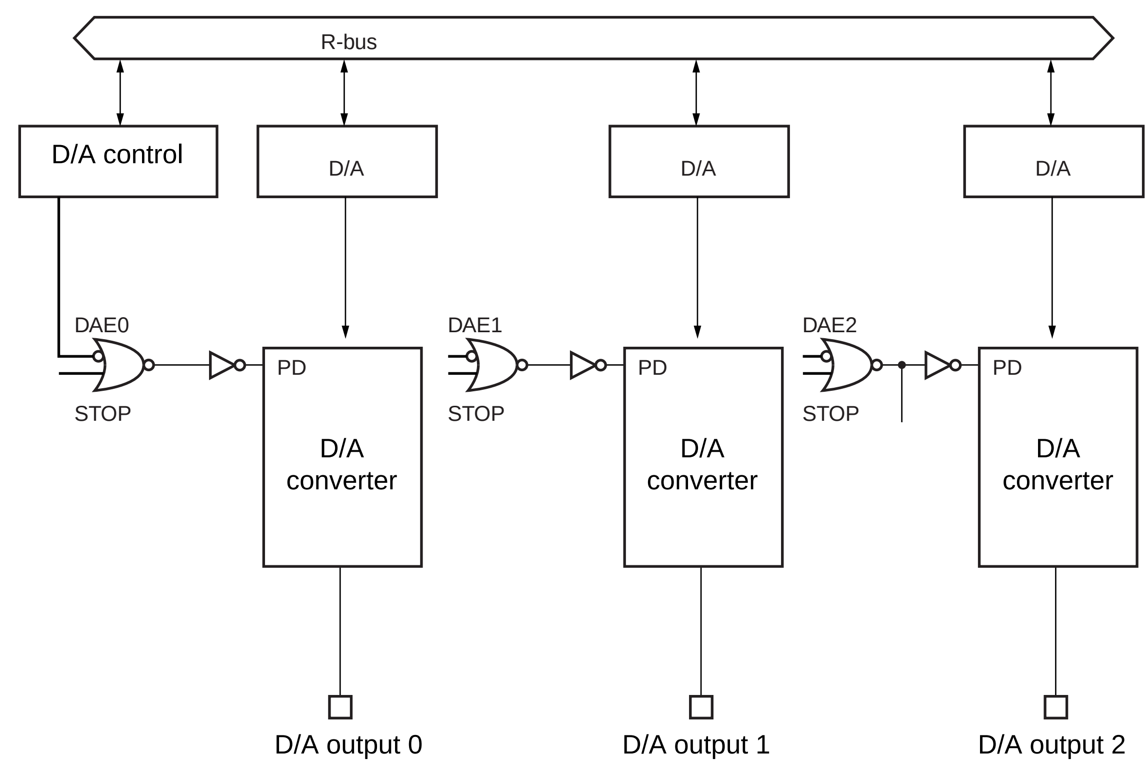
D/A data register 0 to 2(DADR0 to DADR2)

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

D/A control register 0 to 2 (DACR0 to DACR2)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	DAE

(3) Block diagram



16. DMAC (DMA Controller)

(1) Description

This module realize direct memory access (DMA) transfer with the FR family device.
DMA transfer controlled by this module enables many types of data transfer to be performed at high speed without CPU intervention, thereby improving system performance.

• Hardware configuration

This model consists mainly of the following components:

- Independent DMA channels × 5 channels
- 5 channels independent access control circuits
- 32-bit address register (Supports reloading: 2 per channel)
- 16-bit transfer count register (Supports reloading: 1 per channel)
- 4-bit block count register (1 per channel)
- External transfer request input pins: DREQ0, DREQ1, DREQ2 (ch0, ch1, ch2 only)
- External transfer request acceptance output pins: DACK0, DACK1, DACK2 (ch0, ch1,ch2 only)
- DMA end output pins: DEOP0, DEOP1, DEOP2 (ch0, ch1, ch2 only)
- (ch3 only) fly-by transfer (memory to I/O, I/O to memory)
- 2-cycle transfer

• Main function

This module has the following major functions for data transfer:

- Supports independent data transfer for multiple channels (5 channels)

(1) Priority order (ch0 > ch1 > ch2 > ch3 > ch4)

(2) Order can be reversed for ch0 and ch1

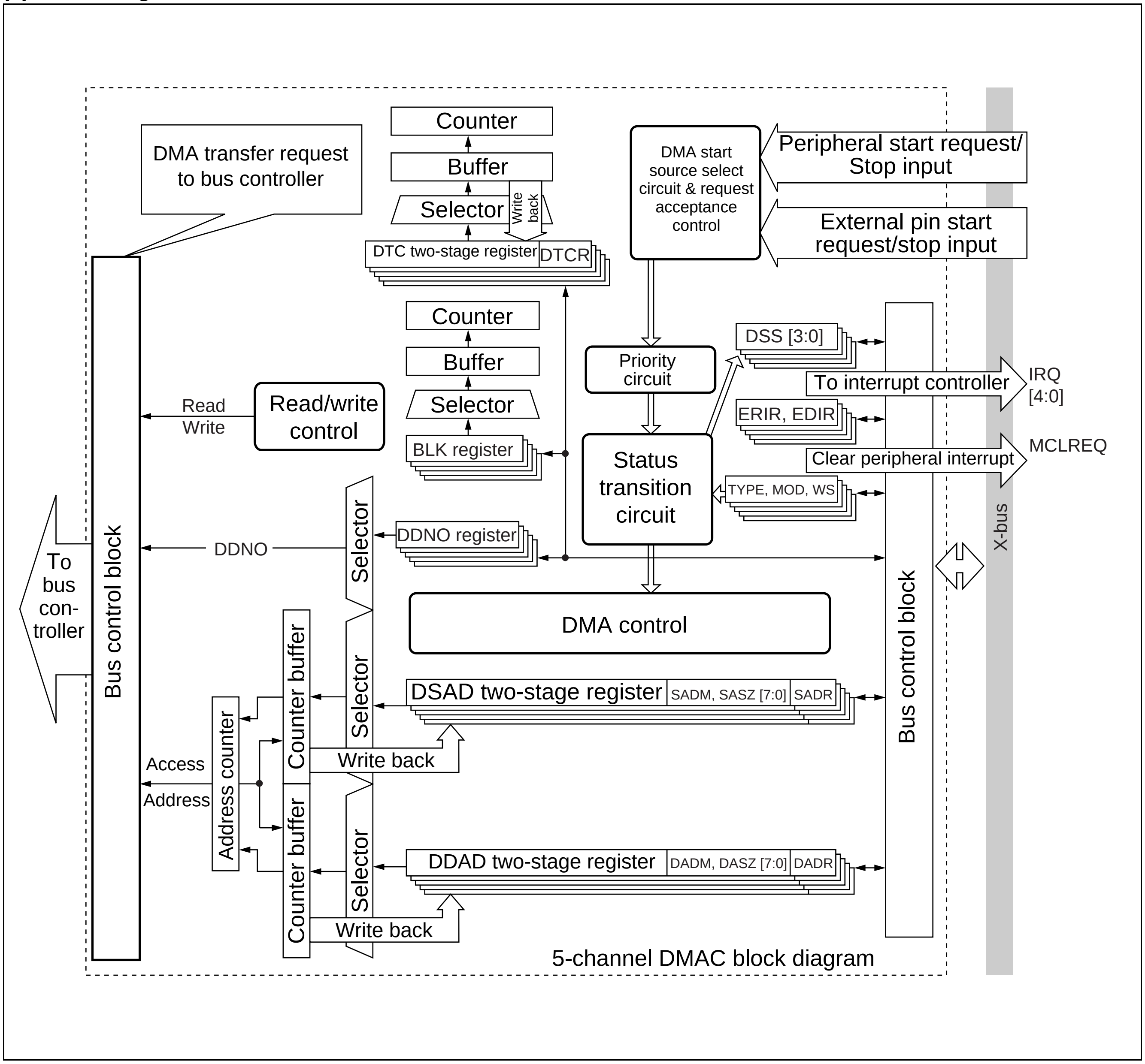
(3) DMAC activation triggers
  - External dedicated pin input (edge detection/level detection: ch0 to ch2 only)
  - Internal peripheral request (Interrupt request sharing, including external interrupts)
  - Software request (register write)

(4) Transmission mode
  - Demand transfer, burst transfer, step transfer, or block transfer
  - Addressing mode: 32-bit full addressing (increment, decrement, or fixed)
    (address increment can be in the range - 255 to + 255)
  - Data length: Byte, halfword, or word
  - Single-shot or reload operation selectable

(2) Register Description

			31 — 16 15 — 0
Ch0 control/status	register A	(DMACA0)	
	register B	(DMACB0)	
Ch1 control/status	register A	(DMACA1)	
	register B	(DMACB1)	
Ch2 control/status	register A	(DMACA2)	
	register B	(DMACB2)	
Ch3 control/status	register A	(DMACA3)	
	register B	(DMACB3)	
Ch4 control/status	register A	(DMACA4)	
	register B	(DMACB4)	
Overall control register		(DMACR)	
Ch0 transfer source address register		(DMASA0)	
		(DMADA0)	
Ch1 transfer source address register		(DMASA1)	
		(DMADA1)	
Ch2 transfer source address register		(DMASA2)	
		(DMADA2)	
Ch3 transfer source address register		(DMASA3)	
		(DMADA3)	
Ch4 transfer source address register		(DMASA4)	
		(DMADA4)	

(3) Block diagram



■ ELECTRICAL CHARACTERISTICS

1. Abusolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Analog power supply voltage*1	DA_{VC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Analog power supply voltage*1	AV_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Analog reference voltage*1	AVRH	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Input voltage*1	V_I	V_{SS} – 0.5	V_{CC} + 0.5	V	*8
Input voltage (Nch open-drain) *1	V_{IND}	V_{SS} – 0.5	V_{SS} + 5.5	V	*8
Analog pin input voltage*1	V_{IA}	V_{SS} – 0.5	AV_{CC} + 0.5	V	*8
Output voltage*1	V_O	V_{SS} – 0.5	V_{CC} + 0.5	V	
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	—	20	mA	*7
“L” level maximum output current	I_{OL}	—	10	mA	*4
“H” level maximum output current (Nch open-drain)	I_{OLND}	—	20	mA	
“L” level average output current	I_{OLAV}	—	8	mA	*5
“H” level average output current (Nch open-drain)	I_{OLAVND}	—	15	mA	
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*6
“H” level maximum output current	I_{OH}	—	– 10	mA	*4
“H” level average output current	I_{OHAV}	—	– 4	mA	*5
“H” level total maximum output current	ΣI_{OH}	—	– 50	mA	
“H” level total average output current	ΣI_{OHAV}	—	– 20	mA	*6
Power consumption	P_D	—	850	mW	
Operating temperature	T_a	– 40	+ 85	°C	
Storage temperature	T_{STG}	—	+ 125	°C	

*1 : The parameter is based on V_{SS} = DA_{VS} = AV_{SS} = 0 V.

*2 : V_{CC} must not be lower than V_{SS} - 0.3 V.

*3 : Be careful not to exceed "V_{CC} + 0.3 V”, for example, when the power is turned on.

*4 : The maximum output current is the peak value for a single pin.

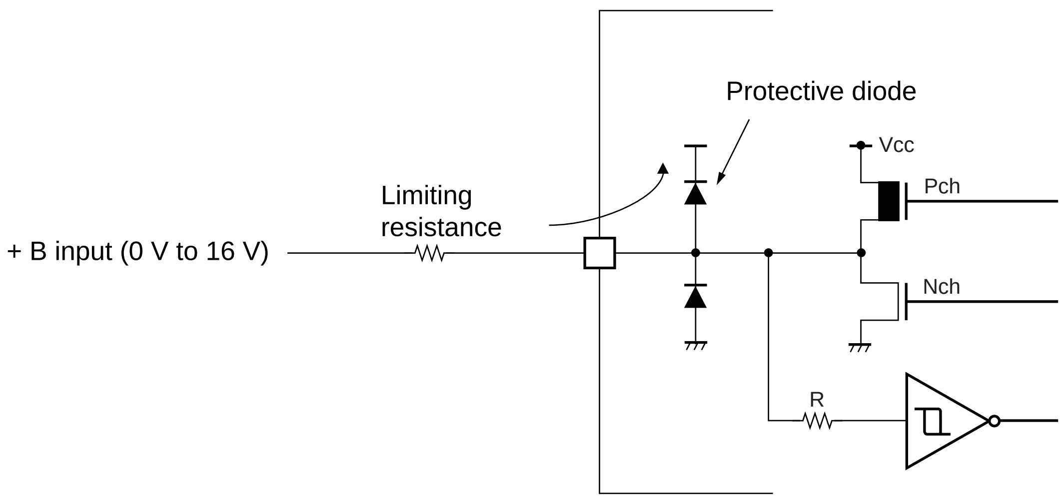
*5 : The average output current is the average current for a single pin over a period of 100 ms.

*6 : The total average output current is the average current for all pins over a period of 100 ms.

*7 : • Relevant pins: Port2, 3, 4, 5, 6, 8, 9, A, B, C, G, H, I, J, K, M, N, O, P, and AN (A/D input)
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that, when the microcontroller drive current is low as in low power consumption mode, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that, if the + B input exists when the microcontroller is off (not fixed at 0 V), power is supplied through the pin, possibly causing the microcontroller to operate imperfectly.
- Note that, if the + B input exists when the power supply is turned on, power is supplied through the pin, possibly resulting in a power-supply voltage at which a power-on reset does not work.
- Be careful not to let the + B input pin open.
- Note that the analog I/O pins (such as the LCD drive and comparator input pins) other than the A/D input pin cannot input + B.

• Sample recommended circuits:

• Input/output equivalent circuits



*8: V_I should not exceed the specified ratings. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = DA_{VS} = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.0	3.6	V	At normal operating
	V_{CC}	3.0	3.6	V	hold RAM status at stop
Analog power supply voltage	DA_{VC}	V_{SS} – 0.3	V_{SS} + 3.6	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6		
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	Ta	– 40	+ 85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Sym-bol	Pin	Conditions	Value Min	Value Typ	Value Max	Unit	Remarks
"H" level input voltage	V_{IH}	Port 2, 3, 4, 5, 6, 9, A, B, C	—	V_{CC} × 0.65	—	V_{CC} − 0.3	V	
	V_{IHS}	Port 8, G, H, I, M, N, O, P, MD0, MD1, MD2, $\overline{INIT}$, $\overline{NMI}$	—	V_{CC} × 0.8	—	V_{CC} − 0.3	V	Hysteresis input
	V_{IHST}	Port J, K, L	—	V_{CC} × 0.8	—	5.25	V	Hysteresis input with stand voltage of 5 V
"L" level input voltage	V_{IL}	Port 2, 3, 4, 5, 6, 9, A, B, C	—	V_{SS}	—	V_{CC} × 0.25	V	
	V_{ILS}	Port 8, G, H, I, M, N, O, P, MD0, MD1, MD2, $\overline{INIT}$, $\overline{NMI}$	—	V_{SS}	—	V_{CC} × 0.2	V	Hysteresis input
	V_{ILST}	Port J, K, L	—	V_{SS}	—	V_{CC} × 0.2	V	Hysteresis input with stand voltage of 5 V
"H" level output voltage	V_{OH}	Port 2, 3, 4, 5, 6, 8, 9, A, B, C, G, H, I, J, K, M, N, O, P	V_{CC} = 3.0 V I_{OH} = − 4.0 mA	V_{CC} − 0.5	—	V_{CC}	V	
"L" level output voltage	V_{OL1}	Port 2, 3, 4, 5, 6, 8, 9, A, B, C, G, H, I, J, K, M, N, O, P	V_{CC} = 3.0 V I_{OL} = 4.0 mA	V_{SS}	—	0.4	V	
	V_{OL2}	Port L	V_{CC} = 3.0 V I_{OL} = 15.0 mA	V_{SS}	—	0.4	V	Nch open-drain
Input leak current (High-Z output Leak-age current)	I_{LI}	All input pin	V_{CC} = 3.6 V $0 < V_I < V_{CC}$	− 5	—	+ 5	µA	
Pull-up resistance	R_{UP}	setting pin $\overline{INIT}$, Pull up	V_{CC} = 3.6 V V_I = 0.45 V	25	50	200	kΩ	

(Continued)

(Continued)

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Sym-bol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	V_{CC}	f_C = 12.5 MHz V_{CC} = 3.3 V	—	160	220	mA	Multiply by 4 CLKB : 50 MHz CLKT : 25 MHz When operating at 25 MHz
	I_{CCS}		f_C = 12.5 MHz V_{CC} = 3.3 V	—	100	140	mA	Sleep When operating at 25 MHz
	I_{CCH}		Ta = + 25 °C V_{CC} = 3.3 V	—	1	100	µA	at stop
	I_{CCL}		Ta = + 25 °C f_C = 32.768 kHz V_{CC} = 3.3 V	—	0.3	3.0	mA	Sub RUN CLKB : 32.768 kHz CLKT : 32.768 kHz When operating at 32.768 kHz
	I_{CCLS}		Ta = + 25 °C f_C = 32.768 kHz V_{CC} = 3.3 V	—	0.2	2.0	mA	Sub sleep When operating at 32.768 kHz
	I_{CCT}		Ta = + 25 °C f_C = 32.768 kHz V_{CC} = 3.3 V	—	5	120	µA	at watch mode operating (Main Off, STOP)
Input capacitance	C_{IH}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, DA_{VC}, DA_{VS}	—	—	5	15	pF	

4. AC Characteristics

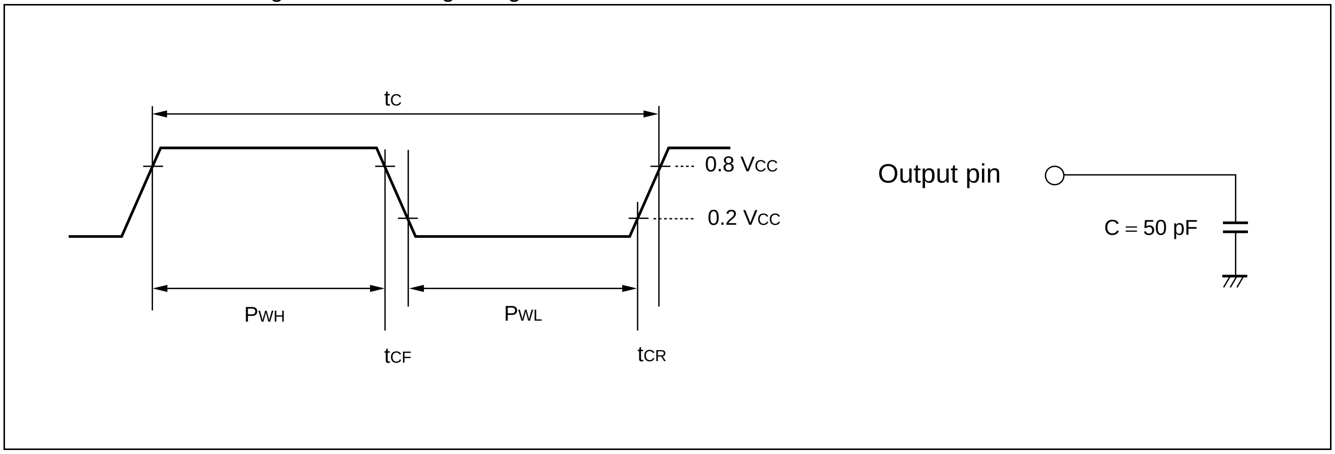
(1) Clock timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

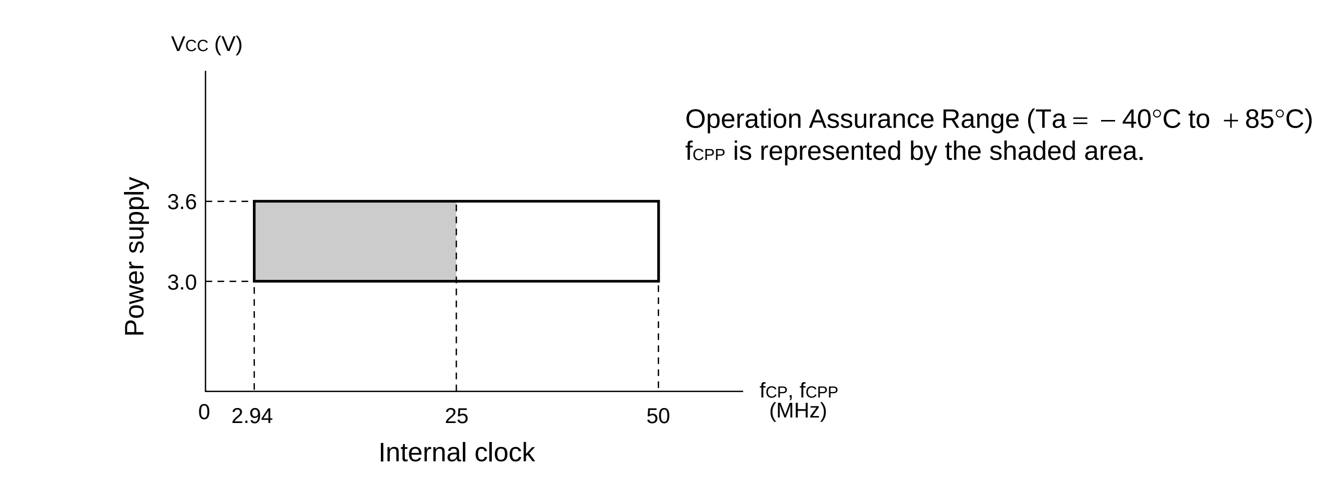
Parameter	Sym-bol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0 X1	—	10	—	12.5	MHz	Main PLL (When operating at max internal frequency (50 MHz) = 12.5 MHz self-oscillation with × 4 PLL)
Clock cycle time	t_C	X0 X1		80	—	100	ns	
Clock frequency	f_C	X0 X1	—	10	—	25	MHz	Main self-oscillation (frequency-halved input)
Internal operating clock frequency	f_{CP}	—	When a minimum value of 12.5 MHz is input as the X0 clock frequency and × 4 multiplication is set for the PLL of the oscillator circuit	2.94*	—	50	MHz	CPU
	f_{CPP}			2.94*	—	25	MHz	Peripheral
	f_{CPT}			2.94*	—	25	MHz	External bus
Internal operating clock cycle time	t_{CP}	—		20	—	340*	ns	CPU
	t_{CPP}			40	—	340*	ns	Peripheral
	t_{CPT}			40	—	340*	ns	External bus
Clock frequency	f_C	X0A X1A	—	30	32.768	35	kHz	SUB self-oscillation
Clock cycle time	t_C	X0A X1A	—	28.6	30.51	33.3	µs	
Input clock palse width	—	X0 X1	P_{WH}/t_C P_{WL}/t_C	40	—	60	%	
Internal operating clock frequency	f_{CP}, f_{CPP}, f_{CPT}	—	When a standard value of 32.768 kHz is input as the X0A clock frequency	2*	—	32	kHz	
Internal operating clock cycle time	t_{CP}, t_{CPP}, t_{CPT}	—		30.51	—	500*	µs	

* : The values assume a gear cycle of 1/16.

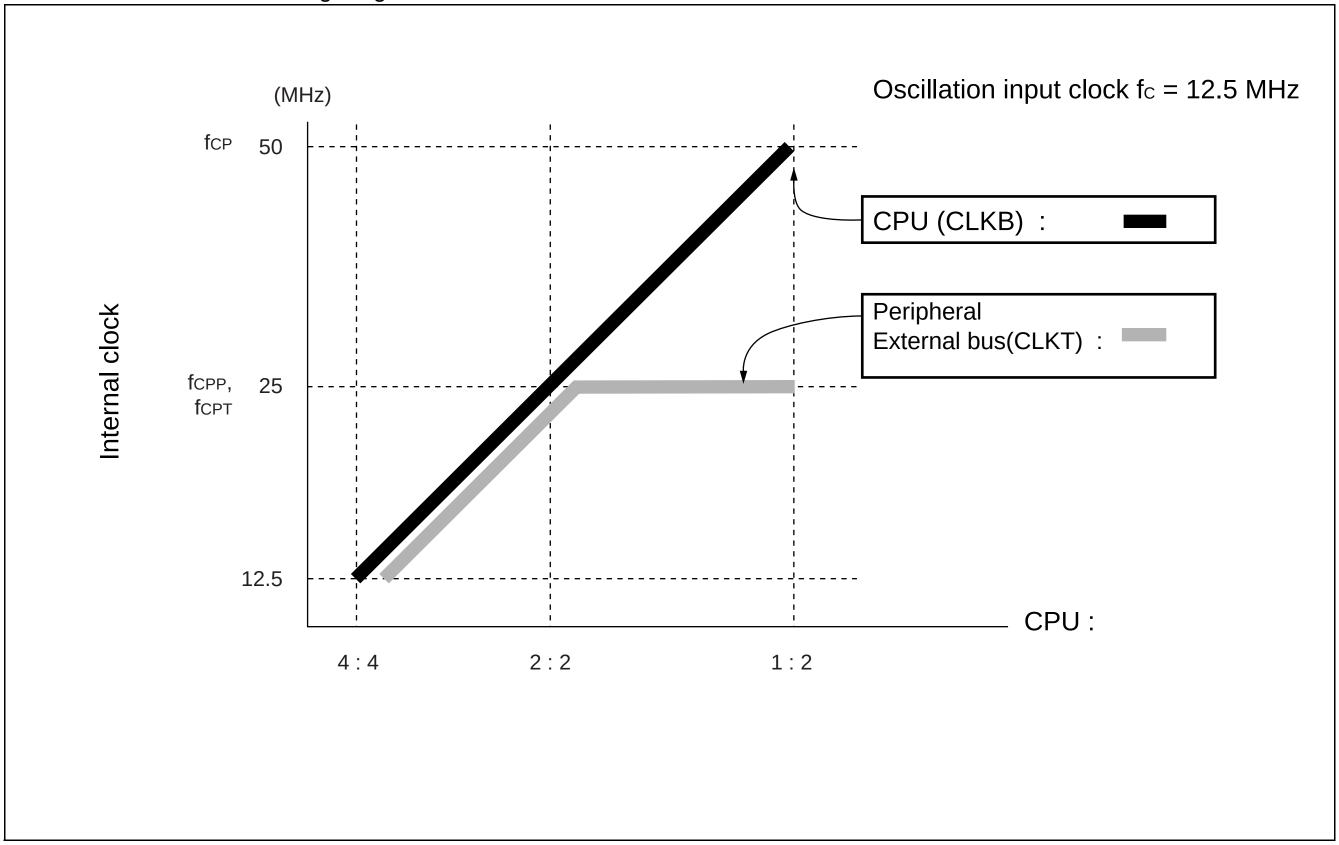
• Conditions for measuring the clock timing ratings



• Operation Assurance Range



• External/internal clock setting range



Notes :
- When the PLL is used, the external clock input must fall between 10.0 and 12.5 MHz.
- Set the PLL oscillation stabilization wait time longer than 454.5 µs. The internal clock gear setting should not exceed the relevant value in the table in “(1) Clock timing ratings”.

(2)Clock output timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Condi-tions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	MCLK, SYSCLK	—	t_{CPT}	—	ns	*1
SYSCLK ↑→ SYSCLK ↓	t_{CHCL}	MCLK, SYSCLK		t_{CYC} − 5	t_{CYC} + 5	ns	*2
SYSCLK ↓→ SYSCLK ↑	t_{CLCH}	MCLK, SYSCLK		t_{CYC} − 5	t_{CYC} + 5	ns	*3

*1 : t_{CYC} is the frequency of one clock cycle after gearing.

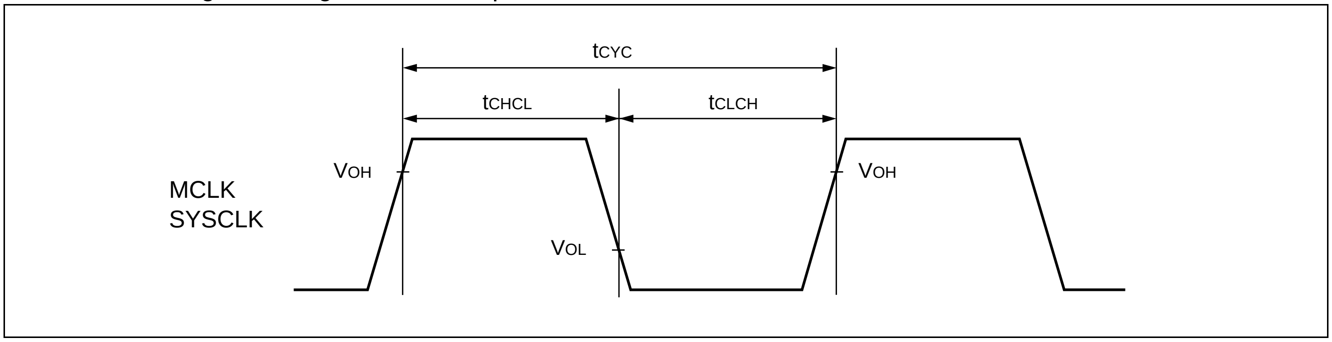
*2 : The following ratings are for the gear ratio set to × 1. For the ratings when the gear ratio is set to between 1/2, 1/4 and 1/8, substitute 1/2, 1/4 or 1/8 for n in the following equation.

$$(1 / 2 \times 1 / n) \times t_{CYC} - 10$$

*3 : The following rating are for the gear ratio set to × 1.

Note : t_{CPT} indicates the internal operating clock cycle time. See “(1) Clock timing”.

In the following AC ratings, MCLK is equivalent to SYSCLK.

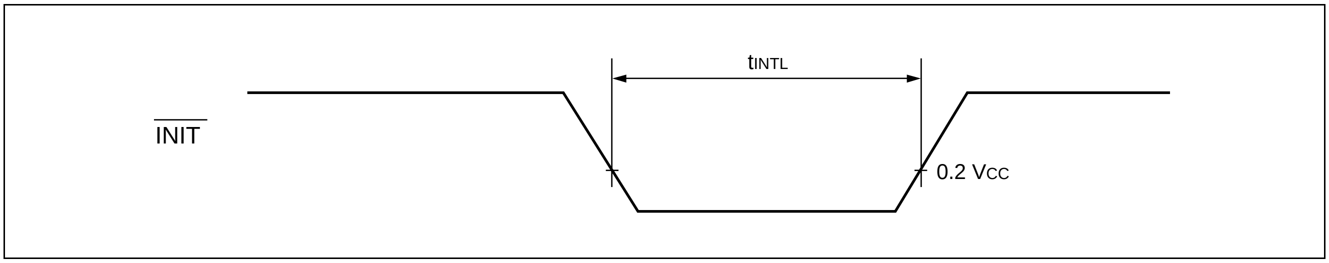


(3) Reset and hardware standby ratings

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Condi-tions	Value		Unit	Remarks
				Min	Max		
$\overline{INIT}$ input time (at power-on)	t_{INTL}	$\overline{INIT}$	—	t_C × 10	—	ns	
$\overline{INIT}$ input time (other than at power-on)				t_C × 10		ns	

Note : t_C indicates the clock cycle time. See “(1) Clock timing”.



(4) Normal bus access read/write operation

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS3}$ setup	t_{CSLCH}	MCLK, $\overline{CS0}$ to $\overline{CS3}$	AWRxL*3 : W02 = 0	3	—	ns	
	t_{CSDLCH}		AWR0L : W02 = 1	− 3	—	ns	
$\overline{CS0}$ to $\overline{CS3}$ hold	t_{CHCSH}		—	3	t_{CYC}/2 + 6	ns	
Address setup	t_{ASCH}	MCLK, A23 to A00		3	—	ns	
	t_{ASWL}	$\overline{WR0}$, $\overline{WR1}$, A23 to A00		3	—	ns	
	t_{ASRL}	$\overline{RD}$, A23 to A00		3	—	ns	
Address hold	t_{CHAX}	MCLK, A23 to A00		3	t_{CYC}/2 + 6	ns	
	t_{WHAX}	$\overline{WR0}$, $\overline{WR1}$, A23 to A00	—	3	—	ns	
	t_{RHAX}	$\overline{RD}$, A23 to A00		3	—	ns	
Valid address → Valid data input time	t_{AVDV}	A23 to A00, D31 to D16		—	3 / 2 × t_{CYC} − 15	ns	*1 *2
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	MCLK, $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWH}			—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		t_{CYC} − 5	—	ns	
Data setup → $\overline{WRx}$ ↑	t_{DSWH}	$\overline{WR0}$, $\overline{WR1}$, D31 to D16		t_{CYC}	—	ns	
$\overline{WRx}$ ↑ → Data hold time	t_{WHDX}			3	—	ns	
$\overline{RD}$ delay time	t_{CHRL}	MCLK, $\overline{RD}$		—	6	ns	
$\overline{RD}$ delay time	t_{CHRH}			—	6	ns	
$\overline{RD}$ ↓ → Valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	t_{CYC} − 10	ns	*1
Data setup →$\overline{RD}$ ↑ Time	t_{DSRH}			10	—	ns	
$\overline{RD}$ ↓ → Data hold time	t_{RHDX}			0	—	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} − 5	—	ns	
$\overline{AS}$ setup	t_{ASLCH}	MCLK, $\overline{AS}$		3	—	ns	
$\overline{AS}$ hold	t_{CHASH}			3	t_{CYC}/2 + 6	ns	

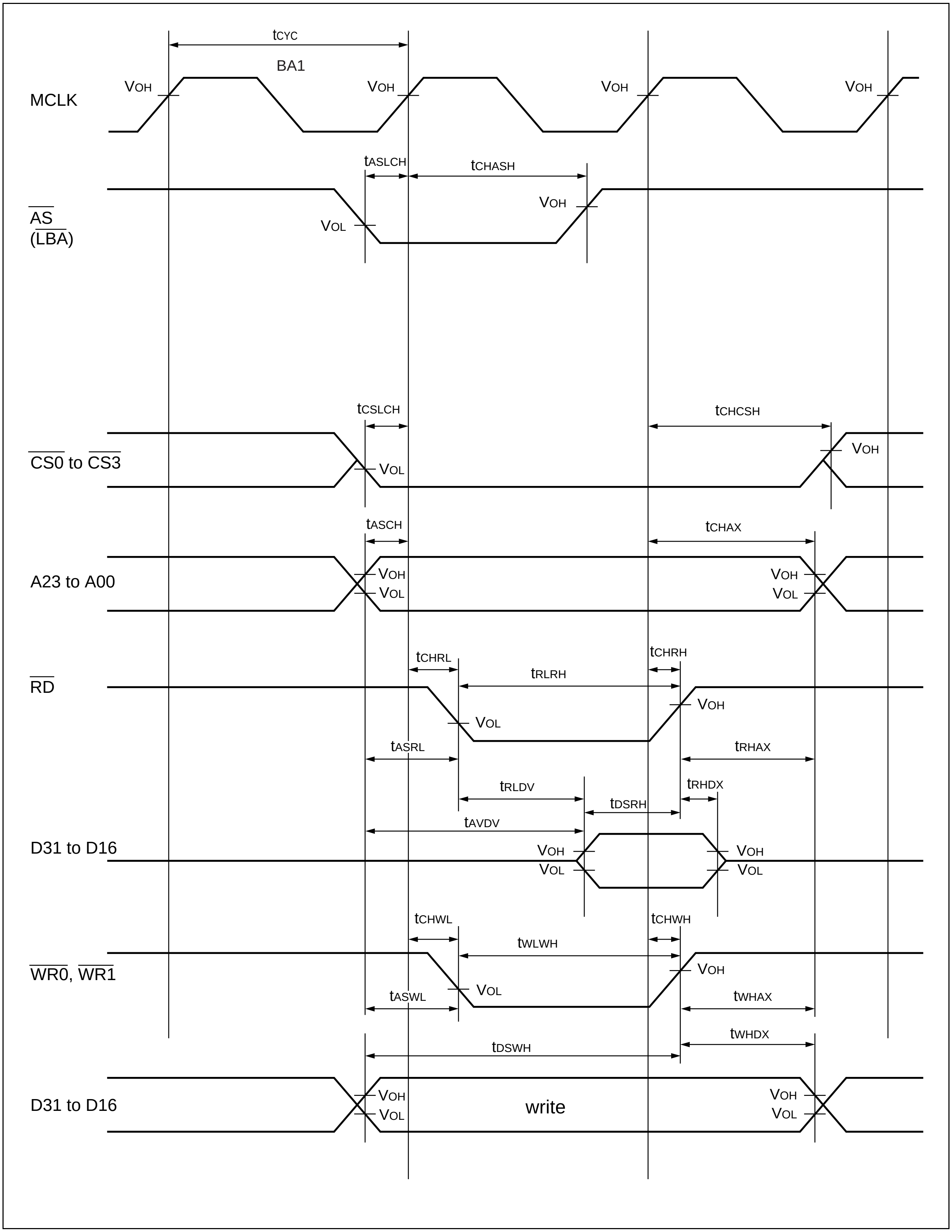
*1 : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{CYC} × the number of cycles added for the delay) to this rating.

*2 : The following ratings are for the gear ratio set to × 1. For the ratings when the gear ratio is set to between 1/2 to 1/16, substitute 1/2 to 1/16 for n in the following equation.

Calculation expression: 3/(2n) × t_{CYC} − 15

*3 : AWRxL : Area Wait Register

Note : t_{CYC} indicates the cycle time. See “(2) Clock output timing”.



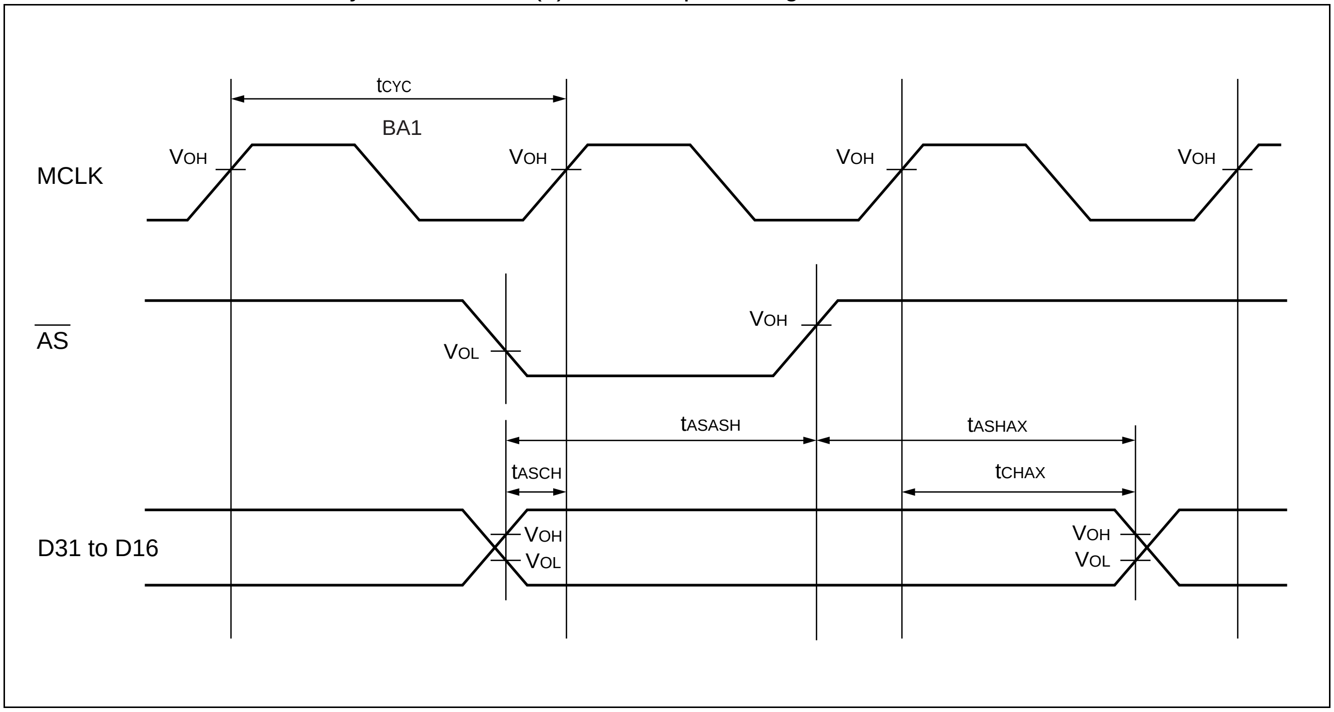
tCYC
BA1
MCLK
VOH
tASLCH
tCHASH
AS
(LBA)
VOL
tCSLCH
tCHCSH
CS0 to CS3
tASCH
tCHAX
A23 to A00
tCHRL
tCHRH
tRLRH
RD
tASRL
tRHAX
tRLDV
tRHDX
tDSRH
tAVDV
D31 to D16
tCHWL
tCHWH
tWLWH
WR0, WR1
tASWL
tWHAX
tWHDX
tDSWH
write

(5) Multiplex bus access read/write operation

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Condi-tions	Value		Unit	Remarks
				Min	Max		
AD15 to AD0 Address AUDI setup time → MCLK ↑	t_{ASCH}	MCLK, D31 to D16	—	3	—	ns	
MCLK ↑ → AD15 to AD0 Address AUDI Hold Time	t_{CHAX}	MCLK, D31 to D16	—	3	$t_{CYC}/2 + 6$	ns	
AD15 to AD0 Address AUDI setup time → $\overline{AS}$ ↑	t_{ASASH}	$\overline{AS}$, D31 to D16	—	12	—	ns	
$\overline{AS}$ ↑ → AD15 to AD0 Address AUDI Hold Time	t_{ASHAX}	$\overline{AS}$, D31 to D16	—	$t_{CYC} - 3$	$t_{CYC} + 3$	ns	

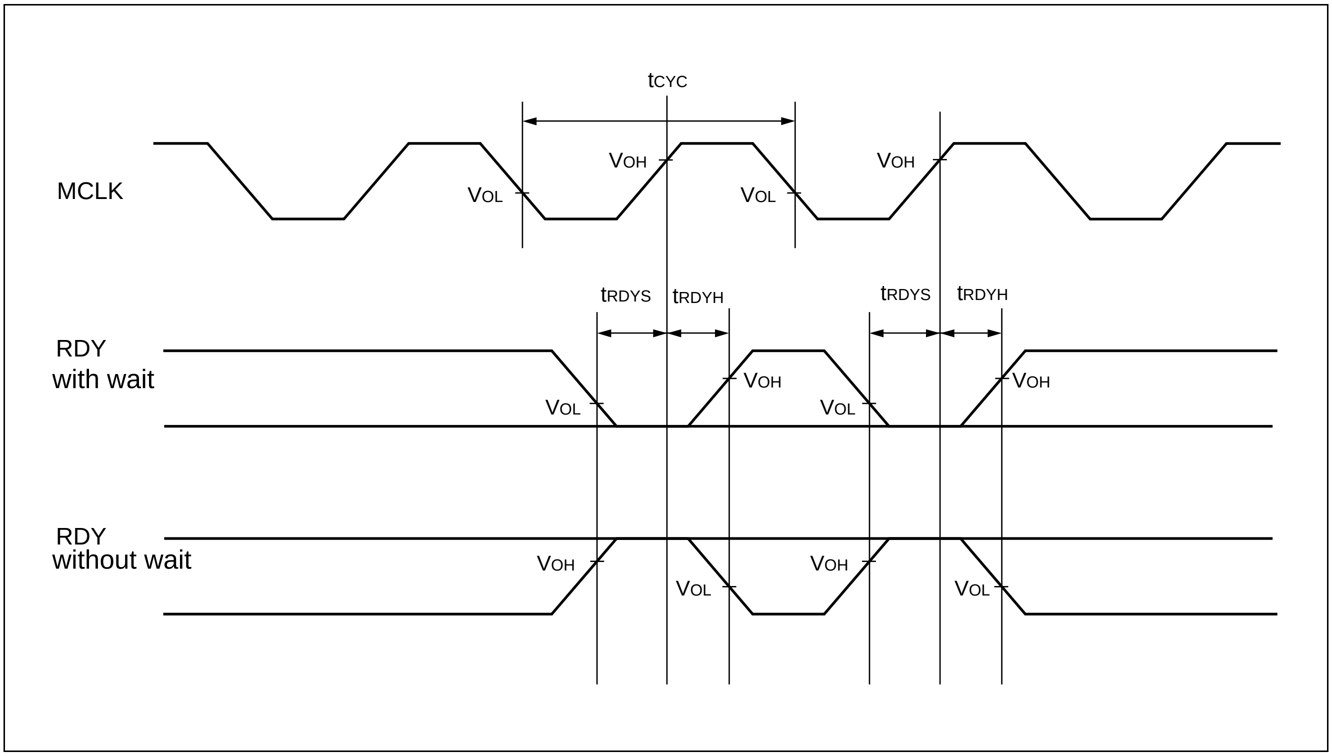
Notes :
- This rating is not guaranteed when the CS→$\overline{RD}$/$\overline{WR}$, and setup delay setting by AWR: bit 1 is “0”.
- Beside This rating, normal bus interface ratings are applicable.
- t_{CYC} indicates the cycle time. See “(2) Clock output timing”.



(6) Ready input timings

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to +85°C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDY setup time → MCLK ↓	t_{RDYS}	MCLK, RDY	—	15	—	ns	
MCLK ↑ → RDY hold time	t_{RDYH}	MCLK, RDY	—	0	—	ns	



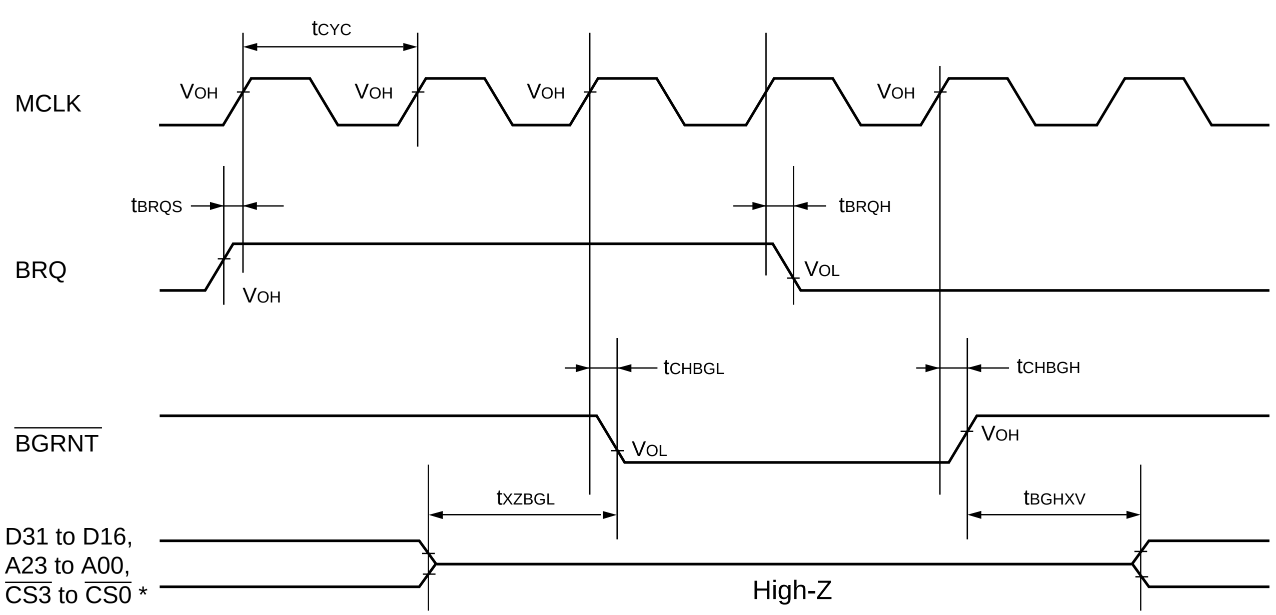
(7) Hold timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DAV_{S} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
BRQ setup time → MCLK ↑	t_{BRQS}	MCLK, BRQ	—	15	—	ns	
MCLK ↑ → BRQ AUDI Hold Time	t_{BRQH}	MCLK, BRQ	—	0	—	ns	
$\overline{BGRNT}$ delay time	t_{CHBGL}	MCLK, $\overline{BGRNT}$	—	$t_{CYC}/2 - 6$	$t_{CYC}/2 + 6$	ns	
$\overline{BGRNT}$ delay time	t_{CHBGH}	MCLK, $\overline{BGRNT}$	—	$t_{CYC}/2 - 6$	$t_{CYC}/2 + 6$	ns	
Pin floating → $\overline{BGRNT}$ ↓ time	t_{XZBGL}	$\overline{BGRNT}$, D31 to D16, A23 to A00, $\overline{CS3}$ to $\overline{CS0}$*	—	$t_{CYC} - 10$	$t_{CYC} + 10$	ns	
$\overline{BGRNT}$ ↑ → Pin valid time	t_{BGHXV}	$\overline{BGRNT}$, D31 to D16, A23 to A00, $\overline{CS3}$ to $\overline{CS0}$*	—	$t_{CYC} - 10$	$t_{CYC} + 10$	ns	

* : These are applied to only the case that SREN bit of area select register (ACR) is set to “1”.

Notes :
- It takes 1 cycle or more from when BRQ is captured until $\overline{BGRNT}$ changes.
- t_{CYC} indicates the cycle time. See “(2) Clock output timing”.



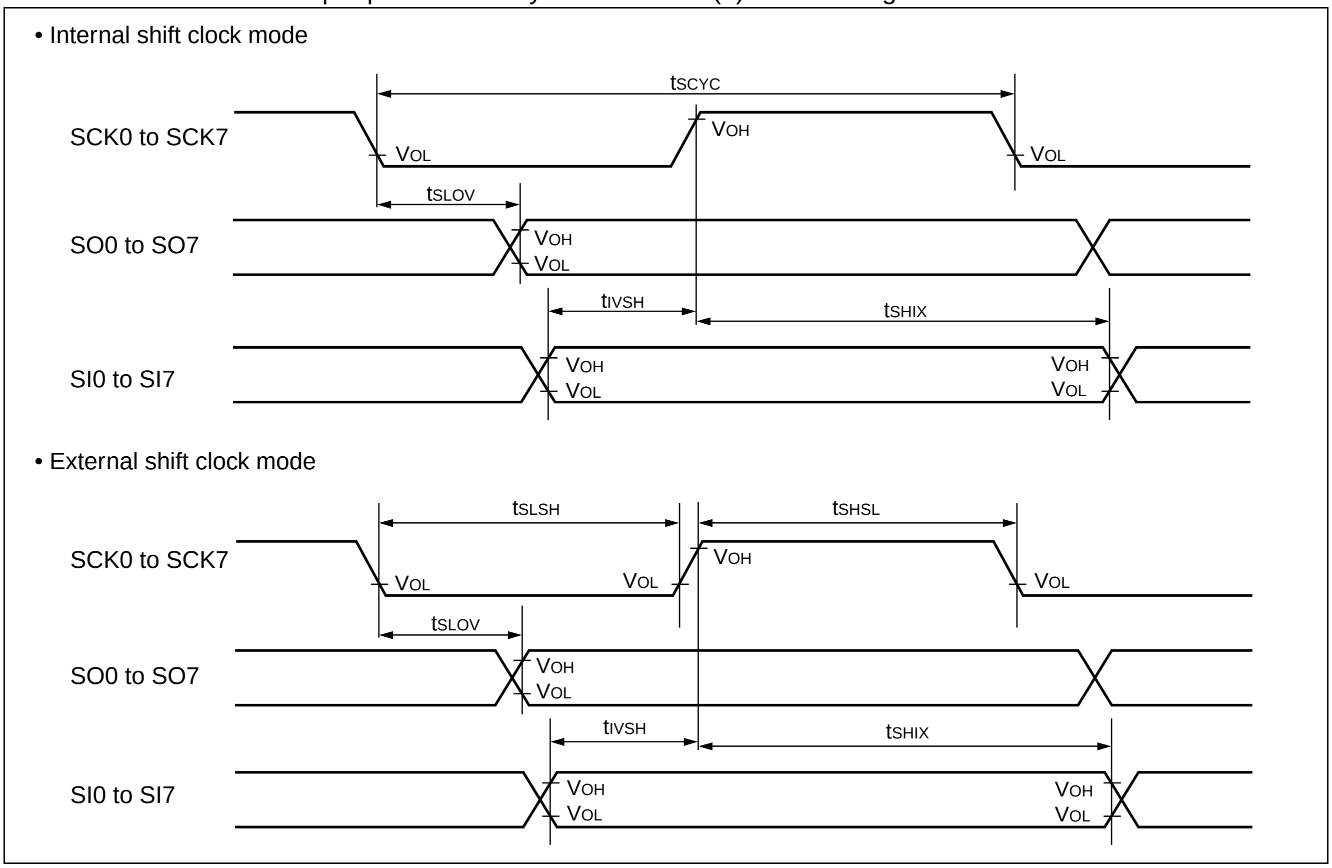
* : These are applied to only the case that SREN bit of area select register (ACR) is set to “1”.

(8) UART, SIO timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK7	Internal shift clock mode	8 t_{CPP}	—	ns	
SCK ↓ → BGRNT delay time	t_{SLOV}	SCK0 to SCK7, SO0 to SO7		− 80	+ 80	ns	
Valid SI → SCK ↑	t_{IVSH}	SCK0 to SCK7, SI0 to SI7		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK7, SI0 to SI7		60	—	ns	
Serial clock H Pulse Width	t_{SHSL}	SCK0 to SCK7	External shift clock mode	4 t_{CPP}	—	ns	
Serial clock L Pulse Width	t_{SLSH}	SCK0 to SCK7		4 t_{CPP}	—	ns	
SCK ↓ → SO delay time	t_{SLOV}	SCK0 to SCK7, SO0 to SO7		—	150	ns	
Valid SI → SCK ↑	t_{IVSH}	SCK0 to SCK7, SI0 to SI7		60	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK7, SI0 to SI7		60	—	ns	

Notes : • Above rating is for CLK synchronous mode.
• t_{CPP} indicates the peripheral clock cycle time. See “(1) Clock timing”.

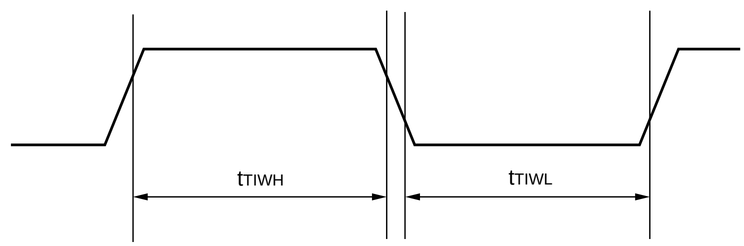


(9) Free-run timer clock, PPG timer input timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	FRCK, TRG0 to TRG5, AIN0 to AIN1, BIN0 to BIN1, ZIN0 to ZIN1	—	2 t_{CPP}	—	ns	

Note : t_{CPP} indicates the peripheral clock cycle time. See “(1) Clock timing”.



(10) Trigger input timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
A/D activation trigger input time	t_{ATGX}	$\overline{ATG}$	—	5 t_{CPP}	—	ns	
input capture input trigger	t_{INP}	IN0 to IN3	—	5 t_{CPP}	—	ns	

Note : t_{CPP} indicates the peripheral clock cycle time. See “(1) Clock timing”.



(11)DMA controller timing

• For edge detection (block/step transfer mode,burst transfer mode)

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DAV_{S} = AV_{SS} = 0 V, Ta = – 40°C to + 85°C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
DREQ Input pulse width	t_{DRWL}	DREQ 0 to DREQ2	—	2 t_{CYC}*	—	ns	
DREQ Input pulse width	t_{DSWH}	DSTP 0 to DSTP2		2 t_{CYC}*	—	ns	

* : t_{CYC} becomes t_{CP} when f_{CPT} is greater than f_{CP}.

• For level detection (demand transfer mode)

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DAV_{S} = AV_{SS} = 0 V, Ta = – 40°C to + 85°C)

Parameter	Symbol	Pin	Condi-tions	Value		Unit	Remarks
				Min	Max		
DREQ setup time	t_{DRS}	MCLK, DREQ 0 to DREQ2	—	15	—	ns	
DREQ Hold Time	t_{DRH}	MCLK, DREQ 0 to DREQ2		0.0	—	ns	
DSTP setup time	t_{DSTPS}	MCLK, DSTP 0 to DSTP2		15	—	ns	
DSTP Hold Time	t_{DSTPH}	MCLK,DSTP 0 to DSTP2		0.0	—	ns	

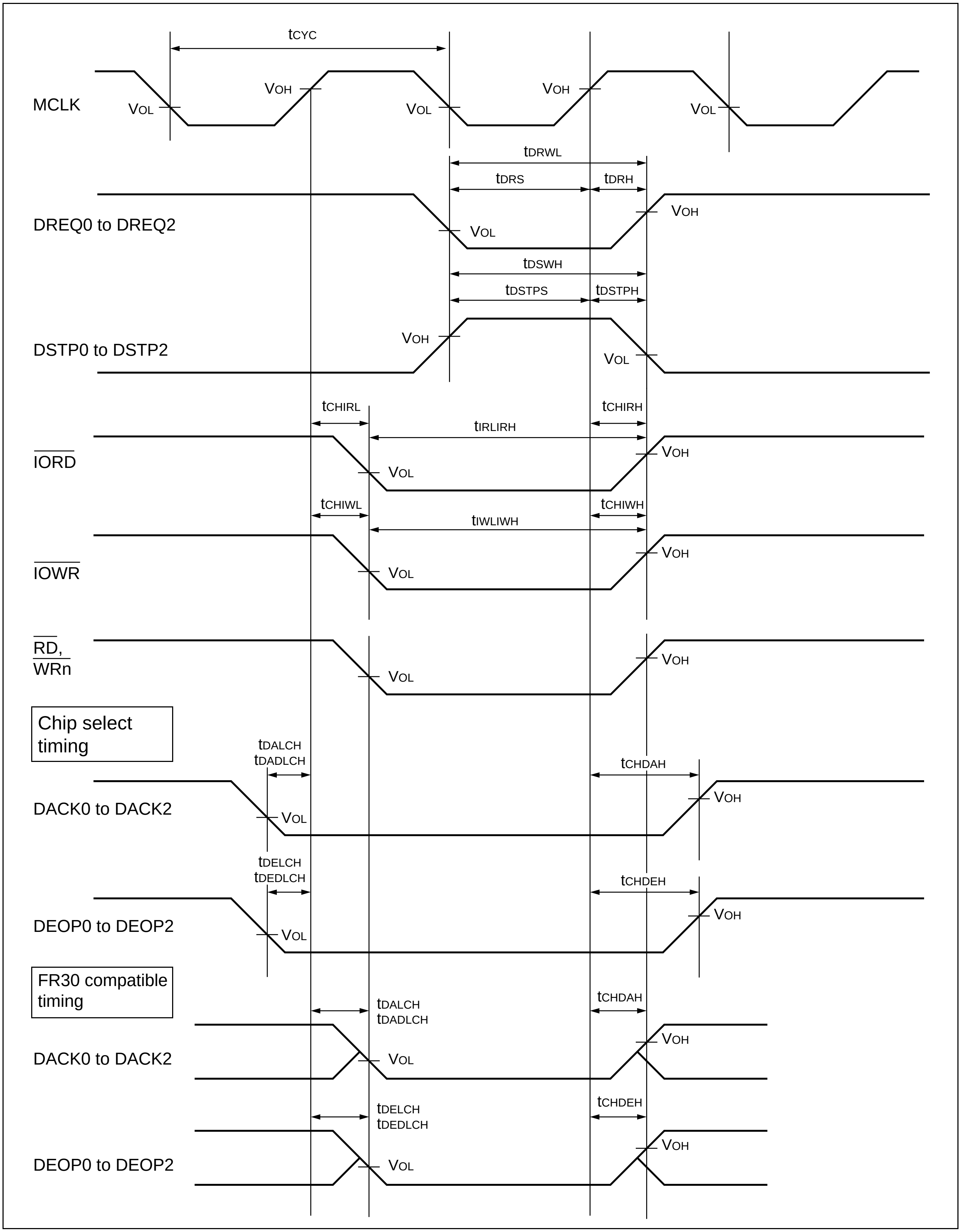
• Common operation mode

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DAV_{S} = AV_{SS} = 0 V, Ta = – 40°C to + 85°C)

Parameter	Symbol	Pin	Condi-tions	Value		Unit	Remarks
				Min	Max		
DACK delay time	t_{DALCH}	MCLK, DACK 0 to DACK2	AWRxL* : W02 = 0	3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{DADLCH}		AWR0L : W02 = 1	– 3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{CHDAH}		—	—	$t_{CYC}/2 + 6$	ns	CS timing
				—	6	ns	FR30 compatible
DEOP delay time	t_{DELCH}	MCLK, DEOP 0 to DEOP2	AWR0L : W02 = 0	3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{DEDLCH}		AWRxL* : W02 = 1	– 3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{CHDEH}		—	—	$t_{CYC}/2 + 6$	ns	CS timing
				—	6	ns	FR30 compatible
$\overline{\text{IORD}}$ delay time	t_{CHIRL}	MCLK, $\overline{\text{IORD}}$	—	—	6	ns	
	t_{CHIRH}			—	6	ns	
$\overline{\text{IOWR}}$ delay time	t_{CHIWL}	MCLK, $\overline{\text{IOWR}}$		—	6	ns	
	t_{CHIWH}			—	6	ns	
$\overline{\text{IORD}}$ minimum pulse width	t_{IRLIRH}	$\overline{\text{IORD}}$		12	—	ns	
$\overline{\text{IOWR}}$ minimum pulse width	t_{IWLIWH}	$\overline{\text{IOWR}}$		12	—	ns	

* : AWRxL: Area Wait Register.

Note : t_{CYC} indicates the cycle time. See “(2) Clock output timing”.


tCYC
MCLK
VOL
VOH
VOL
VOH
VOL
tDRWL
tDRS
tDRH
DREQ0 to DREQ2
VOL
VOH
tDSWH
tDSTPS
tDSTPH
DSTP0 to DSTP2
VOH
VOL
tCHIRL
tCHIRH
tIRLIRH
IORD
VOL
VOH
tCHIWL
tCHIWH
tIWLIWH
IOWR
VOL
VOH
RD,
WRn
VOL
VOH
Chip select timing
tDALCH
tDADLCH
tCHDAH
DACK0 to DACK2
VOL
VOH
tDELCH
tDEDLCH
tCHDEH
DEOP0 to DEOP2
VOL
VOH
FR30 compatible timing
tDALCH
tDADLCH
tCHDAH
DACK0 to DACK2
VOL
VOH
tDELCH
tDEDLCH
tCHDEH
DEOP0 to DEOP2
VOL
VOH

(12) I²C Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DAV_{SS} = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

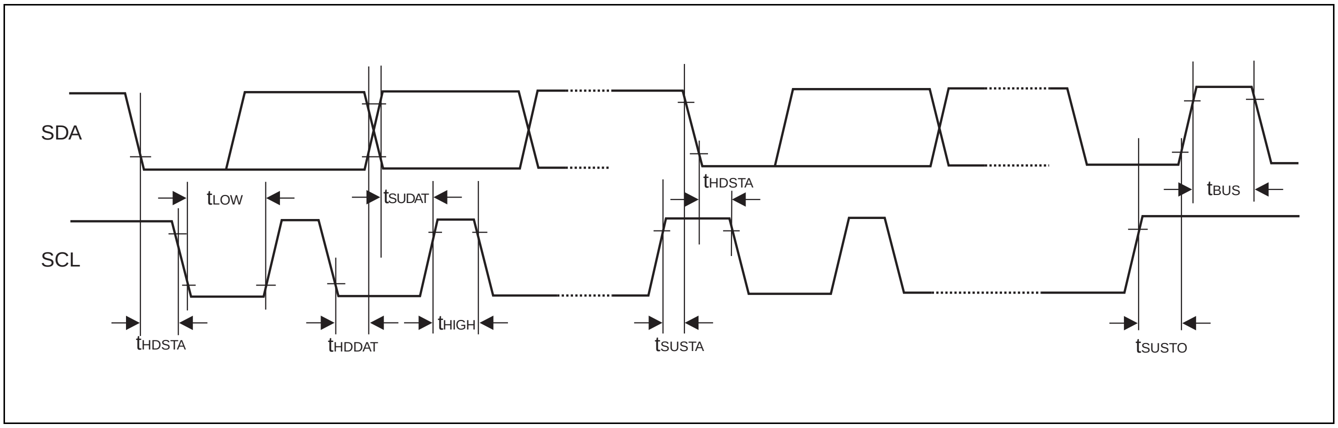
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency*4	f_{SCL}	R = 1.0 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



5. Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = DA_{VS} = AV_{SS} = 0 V, AVRH = 3.0 V to 3.6 V, Ta = − 40°C to + 85°C)

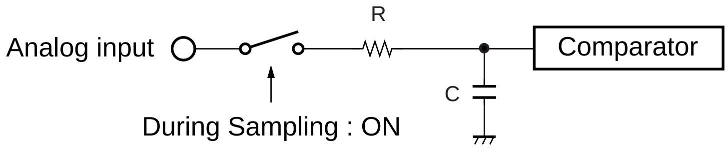
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error*1	—	—	− 5.0	—	+ 5.0	LSB	AVcc = 3.3 V, AVRH = 3.3 V
Nonlinear error*1	—	—	− 3.5	—	+ 3.5	LSB	
Differential linear error*1	—	—	− 2.5	—	+ 2.5	LSB	
Zero transition voltage*1	—	AN11 to AN0	AVRL − 2.0	AVRL + 1.0	AVRL + 6.0	LSB	
Full-transition voltage*1	—	AN11 to AN0	AVRH − 5.5	AVRH + 1.5	AVRH + 3.0	LSB	
Conversion time	—	—	1.48*2	—	300	μs	
Analog power supply current (analog + digital)	I_A	AV_{CC}	—	8	—	mA	
	I_{AH}		—	—	5	μA	At stop
Reference power supply current (between AVRH and AVRL)	I_R	AVRH	—	470	—	μA	AVRH = 3.0 V, AVRL = 0.0 V
	I_{RH}		—	—	10	μA	At stop
Analog input capacitance	—	AN11 to AN0	—	40	—	pF	
Interchannel disparity	—	AN11 to AN0	—	—	4	LSB	

*1: Measured in the CPU sleep state

*2: When the peripheral resource clock frequency is 25.0 MHz, set the Conversion Time Setting Register (ADCT) to a value equal to or greater than 5334_H.
Set each bit as follow :
- Sampling time : SAMP3 to SAMP0 ≥ 5_H
- Conversion time a : CV03 to CV0 ≥ 3_H
- Conversion time b : CV13 to CV0 ≥ 3_H
- Conversion time c : CV23 to CV0 ≥ 4_H

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



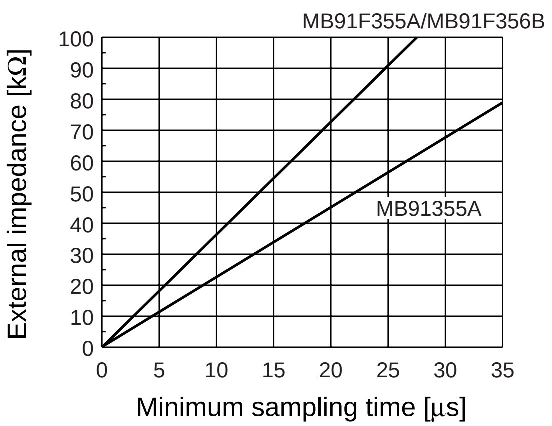
	R	C
MB91355A	0.18 kΩ (Max)	63.0 pF (Max)
MB91F355A	0.18 kΩ (Max)	39.0 pF (Max)
MB91F356B	0.18 kΩ (Max)	39.0 pF (Max)

Note : The values are reference values.

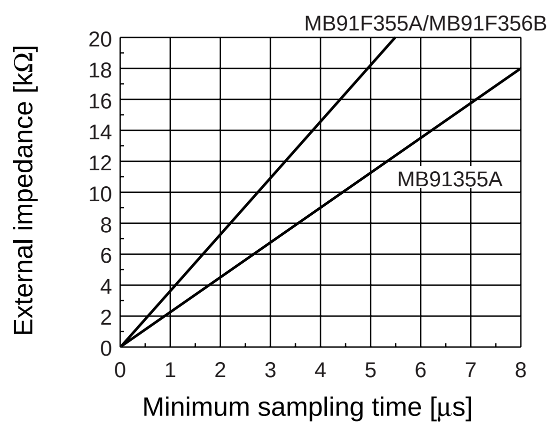
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- **About errors**

As |AVRH-AV_{SS}| becomes smaller, values of relative errors grow larger.

Definition of A/D Converter Terms

- Resolution

  Analog variation that is recognized by an A/D converter.

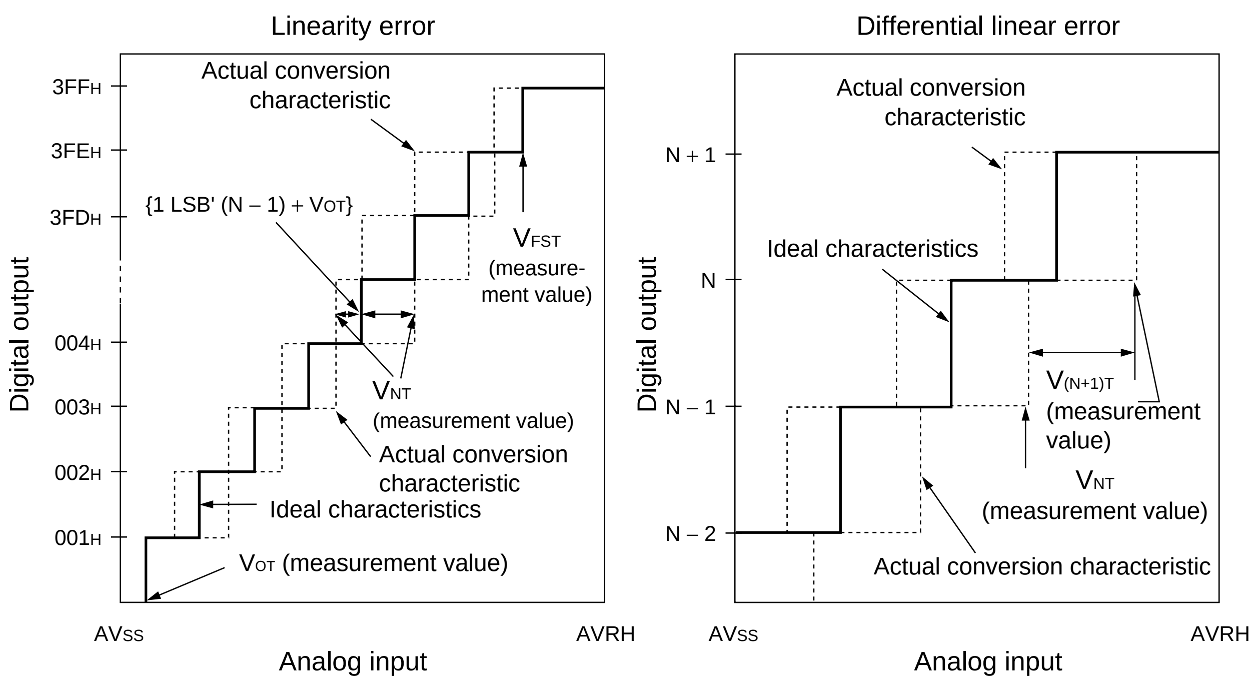
- Linearity error

  Zero transition point ("0000000000" - "0000000001") and full-scale transition point

  Difference between the line connected ("1111111110" - "1111111111") and actual conversion characteristics.

- Differential linear error

  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (N - 1) + \{V_{OT}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB'}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: A voltage at which digital output transitions from $(000)_H$ to $(001)_H$.

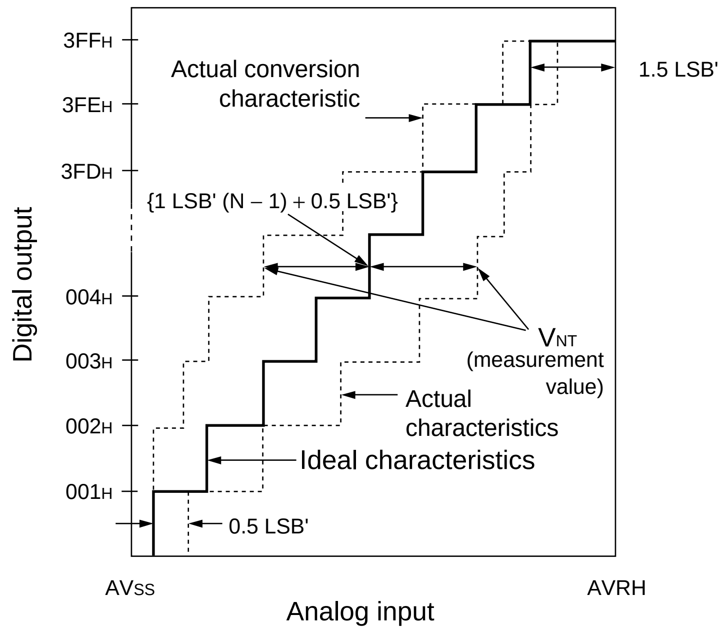
V_{FST}: A voltage at which digital output transitions from $(3FE)_H$ to $(3FF)_H$.

V_{NT}: A voltage at which digital output transitions from (N - 1) to N.

• Total error

This error indicates the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error.

Total error



$$1LS'\text{ (Ideal value) } 1 = \frac{AVRH - AV_{SS}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\text{ LSB'} \times (N - 1) \times \{0.5\text{ LSB'}\}}{1\text{ LSB'}}$$

V_{NT}: A voltage at which digital output transitions from (N + 1) to (N).

V_{OT}’(Ideal value) = AV_{SS} + {0.5 LSB’ [V]

V_{FST}’(Ideal value) = AVRH – 1.5 LSB’ [V]

6. Electrical Characteristics for the D/A Converter

(V_{CC} = DA_{VC} = 3.0 V = 3.6 V, V_{SS} = DA_{VS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	8	bit	
Nonlinear error	—	—	– 2.0	—	+ 2.0	LSB	When the output is unloaded
Differential linear error	—	—	– 1.0	—	+ 1.0	LSB	When the output is unloaded
Convertion speed	—	—	—	0.6	—	µs	When load capacitance (C_L) = 20 pF
	—	—	—	3.0	—	µs	When load capacitance (C_L) = 100 pF
Output high impedance	—	DA0 to DA2	2.0	2.9	3.8	kΩ	
Analog current	—	DA_{VC}	—	40	—	µA	10 µs conversion when the output is unloaded
	I_{ADA}		—	—	460*	µA	Input digital code When fixed at $7A_H$ or 85_H
	I_{ADAH}		—	0.1	—	µA	At power-down

* : This D/A converter varies in current consumption depending on each input digital code.
This rating indicates the current consumption when the digital code that maximizes current consumption is input.

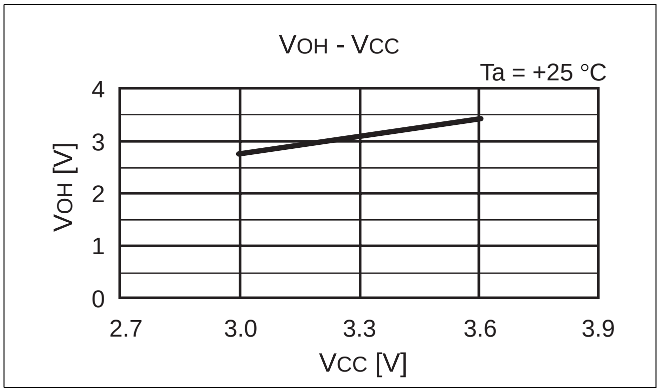
■ FLASH MEMORY WRITE/ERASE CHARACTERISTICS

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Ta = +25 °C, V_{CC} = 3.3 V	—	1	15	s	Excludes 00_H programming prior erasure.
Chip erase time		—	8	—	s	Excludes 00_H programming prior erasure.
Half word (16-bit width) writing time		—	16	3,600	µs	Excludes system-level overhead.
Write/erase cycle	—	—	10,000	—	cycle	
Flash data retention time	Average Ta = +85°C	20	—	—	year	*

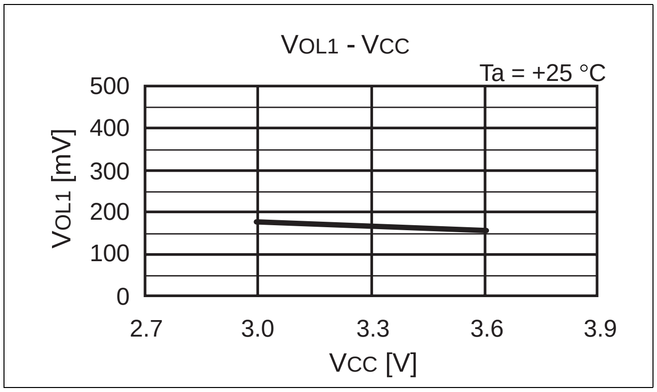
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C).

■ EXAMPLE CHARACTERISTICS

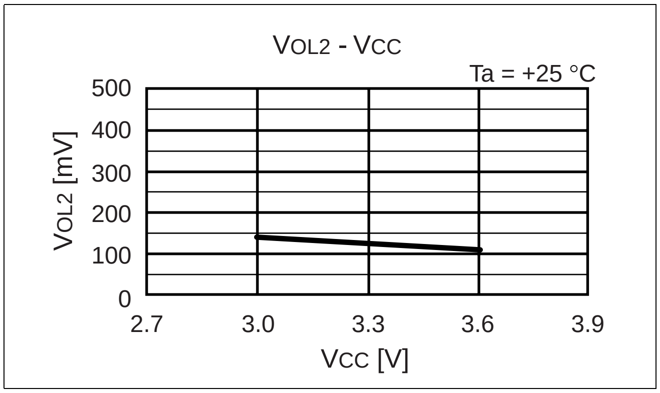
(1) "H" level output voltage



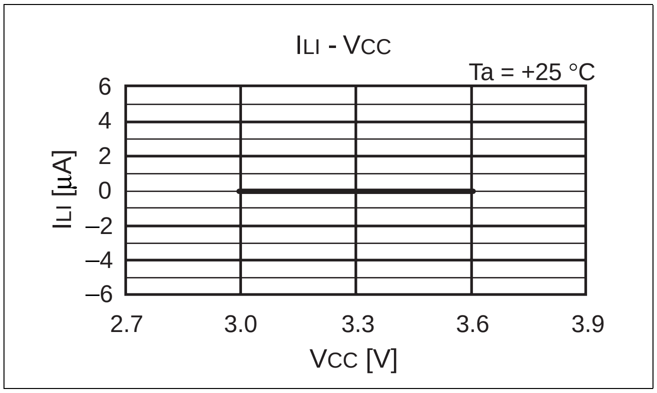
(2) "L" level output voltage



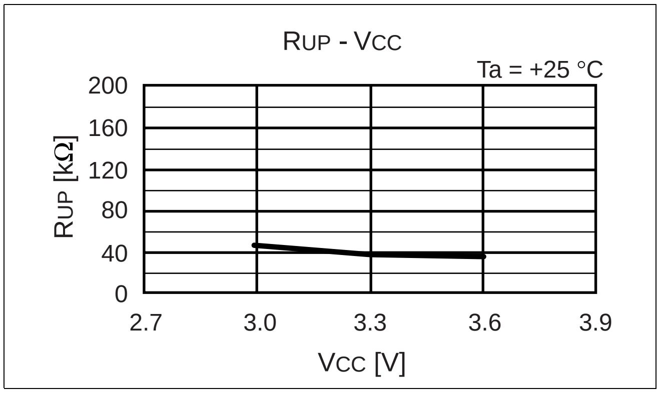
(3) "L" level output voltage (Nch open-drain)



(4) Input leak current

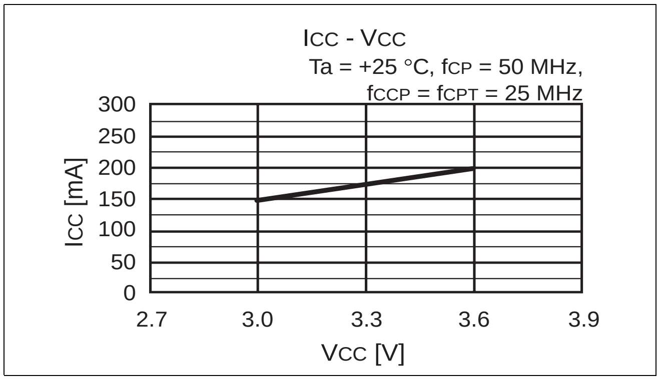


(5) Pull-up resistance

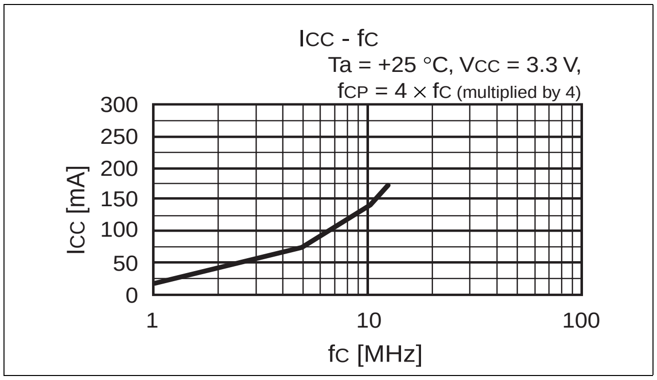


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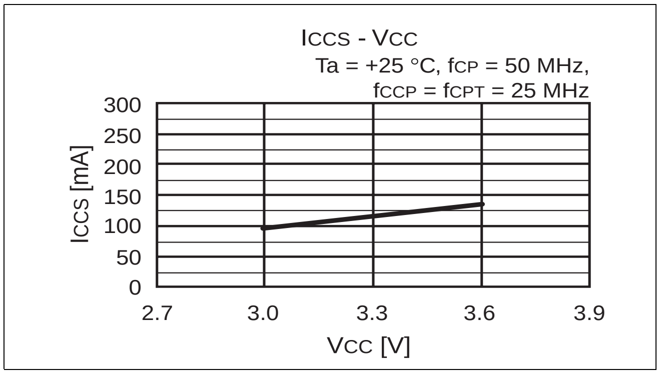
(6) Power supply current



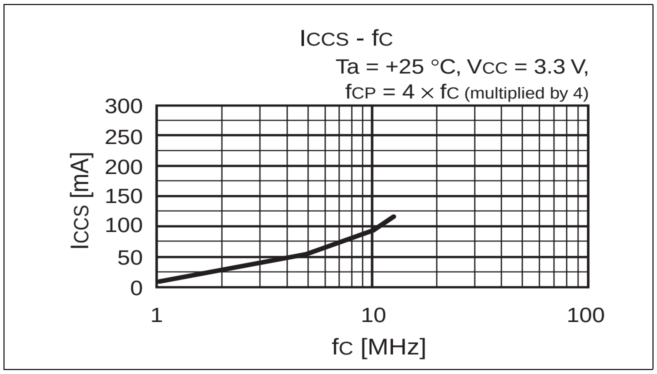
(7) Power supply current



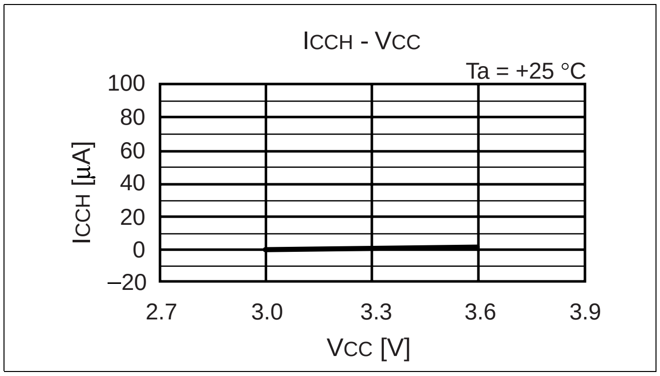
(8) Power supply current at sleep



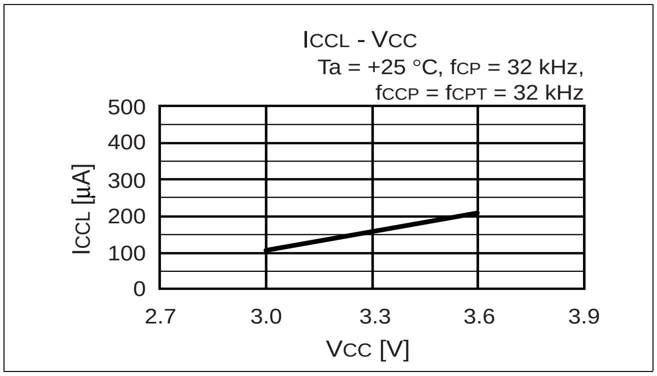
(9) Power supply current at sleep



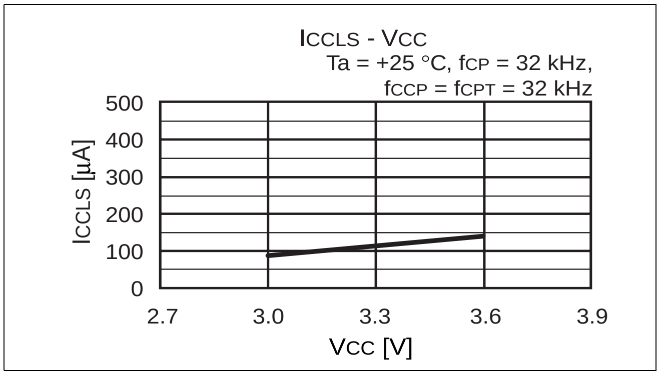
(10) Power supply current at stop



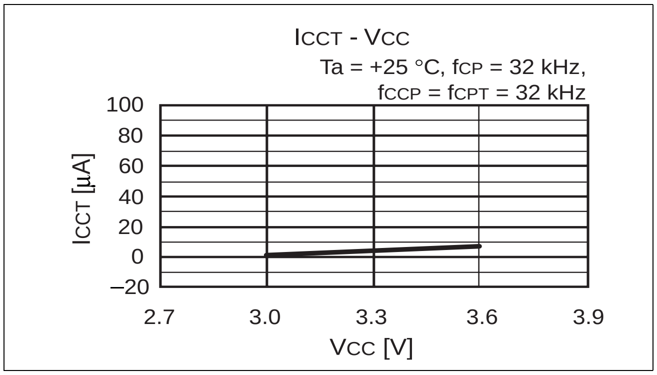
(11) Sub RUN power supply current



(12) Sub sleep power supply current



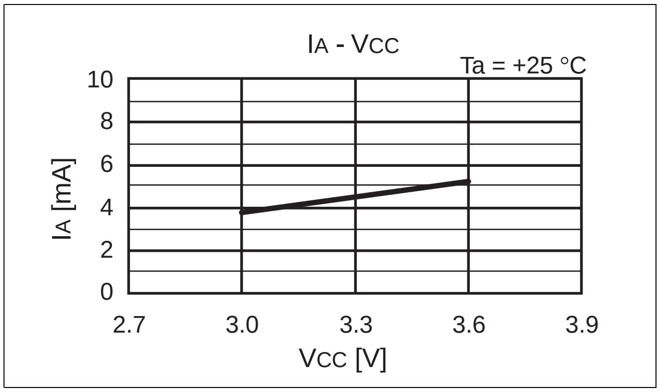
(13) Watch mode power supply current



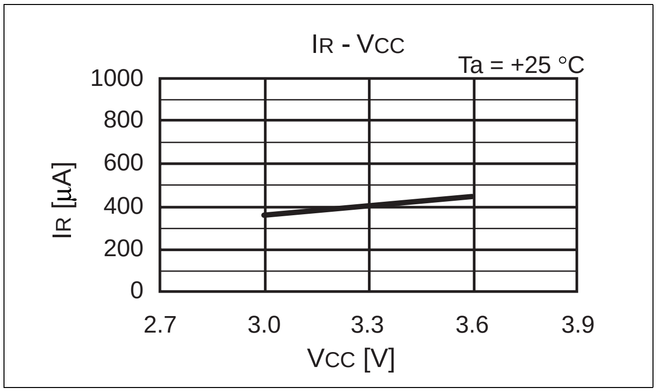
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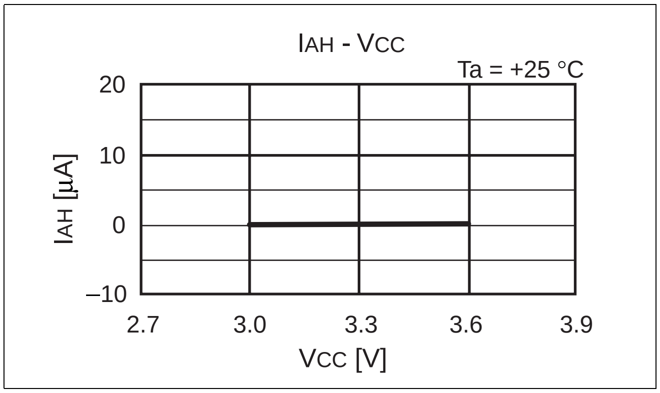
(14) A/D converter power supply current



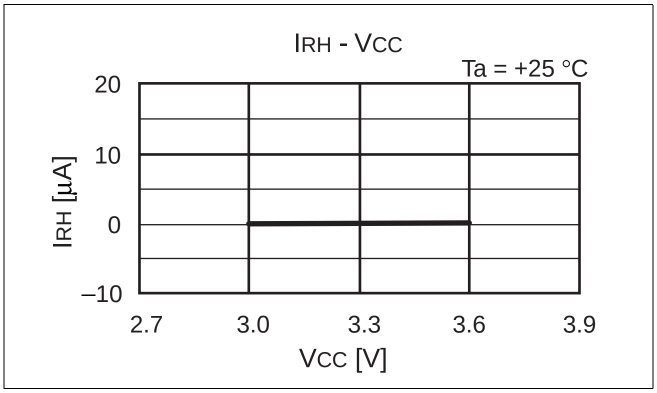
(15) A/D converter reference power supply voltage



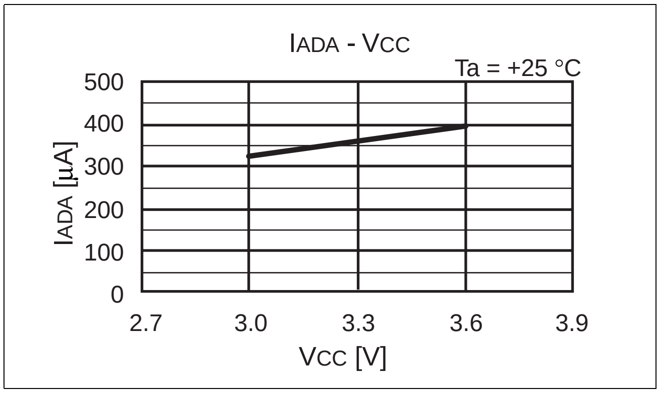
(16) A/D converter power supply current at stop



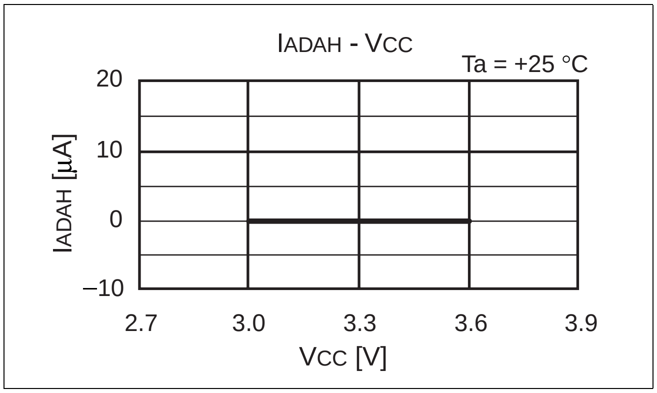
(17) A/D converter reference power supply current at stop



(18) D/A converter power supply current
< per 1 channel >



(19) D/A converter power supply current at power down



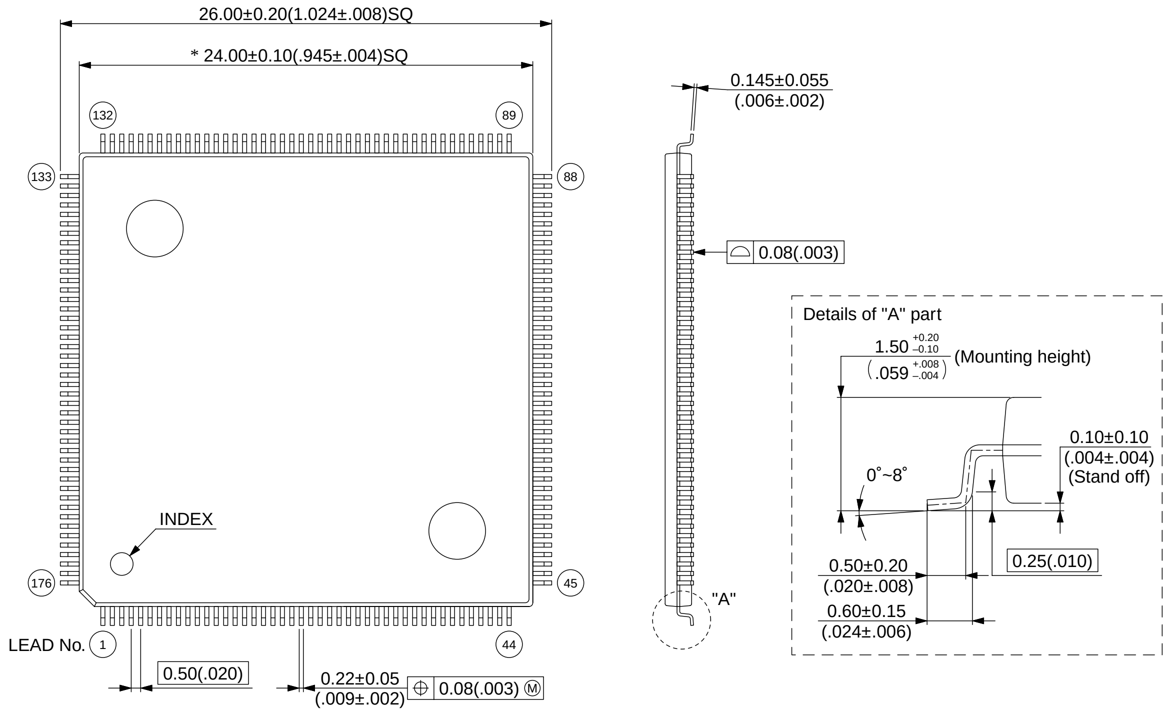
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91F355APMT-002	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91F356BPMT	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91355APMT	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91354APMT	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package

■ PACKAGE DIMENSION

176-pin plastic LQFP
(FPT-176P-M02)

Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25 (.010) Max (each side) .
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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